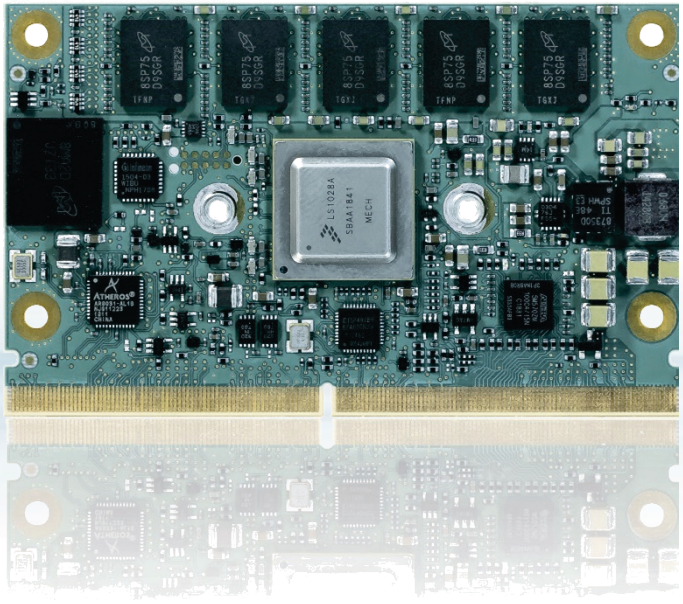
USER GUIDE



# SMARC-sAL28

User Guide Rev. 1.1

Doc-ID: 1064-6120

POSSIBILITIES START HERE kontron S&T Group

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# SMARC-SAL28 – USER GUIDE

## Disclaimer

Kontron would like to point out that the information contained in this manual may be subject to alteration, particularly as a result of the constant upgrading of Kontron products. This document does not entail any guarantee on the part of Kontron with respect to technical processes described in the manual or any product characteristics set out in the manual. Kontron assumes no responsibility or liability for the use of the described product(s), conveys no license or title under any patent, copyright or mask work rights to these products and makes no representations or warranties that these products are free from patent, copyright or mask work right infringement unless otherwise specified. Applications that are described in this manual are for illustration purposes only. Kontron makes no representation or warranty that such application will be suitable for the specified use without further testing or modification. Kontron expressly informs the user that this manual only contains a general description of processes and instructions which may not be applicable in every individual case. In cases of doubt, please contact Kontron.



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# Revision History

| Revision | Brief Description of Changes | Date of Issue | Author |
|---|---|---|---|
| 1.0 | Initial issue | 2020-January-20 | hjs |
| 1.1 | Word2016 issues | 2021-March-31 | hjs |

# Intended Use

**THIS DEVICE AND ASSOCIATED SOFTWARE ARE NOT DESIGNED, MANUFACTURED OR INTENDED FOR USE OR RESALE FOR THE OPERATION OF NUCLEAR FACILITIES, THE NAVIGATION, CONTROL OR COMMUNICATION SYSTEMS FOR AIRCRAFT OR OTHER TRANSPORTATION, AIR TRAFFIC CONTROL, LIFE SUPPORT OR LIFE SUSTAINING APPLICATIONS, WEAPONS SYSTEMS, OR ANY OTHER APPLICATION IN A HAZARDOUS ENVIRONMENT, OR REQUIRING FAIL-SAFE PERFORMANCE, OR IN WHICH THE FAILURE OF PRODUCTS COULD LEAD DIRECTLY TO DEATH, PERSONAL INJURY, OR SEVERE PHYSICAL OR ENVIRONMENTAL DAMAGE (COLLECTIVELY, "HIGH RISK APPLICATIONS").**

You understand and agree that your use of Kontron devices as a component in High Risk Applications is entirely at your risk. To minimize the risks associated with your products and applications, you should provide adequate design and operating safeguards. You are solely responsible for compliance with all legal, regulatory, safety, and security related requirements concerning your products. You are responsible to ensure that your systems (and any Kontron hardware or software components incorporated in your systems) meet all applicable requirements. Unless otherwise stated in the product documentation, the Kontron device is not provided with error-tolerance capabilities and cannot therefore be deemed as being engineered, manufactured or setup to be compliant for implementation or for resale as device in High Risk Applications. All application and safety related information in this document (including application descriptions, suggested safety measures, suggested Kontron products, and other materials) is provided for reference only.

**⚠CAUTION**

**Handling and operation of the product is permitted only for trained personnel within a work place that is access controlled. Please follow the "General Safety Instructions" supplied with the system.**

***NOTICE***

**You find the most recent version of the "General Safety Instructions" online in the download area of this product.**

## Customer Support

Find Kontron contacts by visiting: http://www.kontron.com/support.

## Terms and Conditions

Kontron warrants products in accordance with defined regional warranty periods. For more information about warranty compliance and conformity, and the warranty period in your region, visit http://www.kontron.com/terms-and-conditions.

Kontron sells products worldwide and declares regional General Terms & Conditions of Sale, and Purchase Order Terms & Conditions. Visit http://www.kontron.com/terms-and-conditions.

For contact information, refer to the corporate offices contact information on the last page of this user guide or visit our website CONTACT US.

## Customer Support

Find Kontron contacts by visiting: https://www.kontron.de/support-and-services.

## Customer Service

As a trusted technology innovator and global solutions provider, Kontron extends its embedded market strengths into a services portfolio allowing companies to break the barriers of traditional product lifecycles. Proven product expertise coupled with collaborative and highly-experienced support enables Kontron to provide exceptional peace of mind to build and maintain successful products.

For more details on Kontron's service offerings such as: enhanced repair services, extended warranty, Kontron training academy, and more visit http://www.kontron.com/support-and-services/services.

## Customer Comments

If you have any difficulties using this user guide, discover an error, or just want to provide some feedback, contact Kontron support. Detail any errors you find. We will correct the errors or problems as soon as possible and post the revised user guide on our website.

# Symbols

The following symbols may be used in this manual

| | |
|---|---|
| **⚠DANGER** | DANGER indicates a hazardous situation which, if not avoided, will result in death or serious injury. |
| **⚠WARNING** | WARNING indicates a hazardous situation which, if not avoided, could result in death or serious injury. |
| ***NOTICE*** | NOTICE indicates a property damage message. |
| **⚠CAUTION** | CAUTION indicates a hazardous situation which, if not avoided, may result in minor or moderate injury. |
|  | Electric Shock!<br>This symbol and title warn of hazards due to electrical shocks (> 60 V) when touching products or parts of products. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your material. |
|  | ESD Sensitive Device!<br>This symbol and title inform that the electronic boards and their components are sensitive to static electricity. Care must therefore be taken during all handling operations and inspections of this product in order to ensure product integrity at all times. |
|  | HOT Surface!<br>Do NOT touch! Allow to cool before servicing. |
|  | Laser!<br>This symbol inform of the risk of exposure to laser beam and light emitting devices (LEDs) from an electrical device. Eye protection per manufacturer notice shall review before servicing. |
|  | This symbol indicates general information about the product and the user guide.<br>This symbol also indicates detail information about the specific product configuration. |
|  | This symbol precedes helpful hints and tips for daily use. |

# For Your Safety

Your new Kontron product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new Kontron product, you are requested to conform with the following guidelines.

## High Voltage Safety Instructions

As a precaution and in case of danger, the power connector must be easily accessible. The power connector is the product's main disconnect device.

**⚠CAUTION**

Warning

**All operations on this product must be carried out by sufficiently skilled personnel only.**

**⚠CAUTION**

Electric Shock!

**Before installing a non hot-swappable Kontron product into a system always ensure that your mains power is switched off. This also applies to the installation of piggybacks. Serious electrical shock hazards can exist during all installation, repair, and maintenance operations on this product. Therefore, always unplug the power cable and any other cables which provide external voltages before performing any work on this product.**

**Earth ground connection to vehicle's chassis or a central grounding point shall remain connected. The earth ground cable shall be the last cable to be disconnected or the first cable to be connected when performing installation or removal procedures on this product.**

## Special Handling and Unpacking Instruction

***NOTICE***

ESD Sensitive Device!

**Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.**

Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the product is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the product.

# General Instructions on Usage

In order to maintain Kontron's product warranty, this product must not be altered or modified in any way. Changes or modifications to the product, that are not explicitly approved by Kontron and described in this User Guide or received from Kontron's Technical Support as a special handling instruction, will void your warranty.

This product should only be installed in or connected to systems that meet all necessary technical and specific environmental requirements. This also applies to the operational temperature range of the specific board version, which must not be exceeded. If batteries are present, their temperature restrictions must be taken into account.

In performing all necessary installation and application operations, only follow the instructions supplied by the present User Guide.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the product then re-pack it in the same manner as it was delivered.

Special care is necessary when handling or unpacking the product. See Special Handling and Unpacking Instruction.

# Quality and Environmental Management

Kontron aims to deliver reliable high-end products designed and built for quality, and aims to complying with environmental laws, regulations, and other environmentally oriented requirements. For more information regarding Kontron's quality and environmental responsibilities, visit http://www.kontron.com/about-kontron/corporate-responsibility/quality-management.

## Disposal and Recycling

Kontron's products are manufactured to satisfy environmental protection requirements where possible. Many of the components used are capable of being recycled. Final disposal of this product after its service life must be accomplished in accordance with applicable country, state, or local laws or regulations.

## WEEE Compliance

The Waste Electrical and Electronic Equipment (WEEE) Directive aims to:

Reduce waste arising from electrical and electronic equipment (EEE)

Make producers of EEE responsible for the environmental impact of their products, especially when the product become waste

Encourage separate collection and subsequent treatment, reuse, recovery, recycling and sound environmental disposal of EEE

Improve the environmental performance of all those involved during the lifecycle of EEE

**Environmental protection is a high priority with Kontron.**
**Kontron follows the WEEE directive**
**You are encouraged to return our products for proper disposal.**

# Table of Contents

# List of Tables

# List of Figures

# 1/ Introduction

This manual describes the Smart Mobility Architecture (SMARC) sAL28 (NXP LS1028) board. The Advanced RISC Machines (ARM) based module is equipped with a NXP i.MX7 processor. The dual core SoC take advantage of the optimized power consumption and performance ratio.

The use of this Users Guide implies a basic knowledge of PC hard- and software. This manual is focussed on describing the special features and is not intended to be a standard PC textbook. New users are recommended to study the short installation procedure stated in the following chapter before switching on the power.

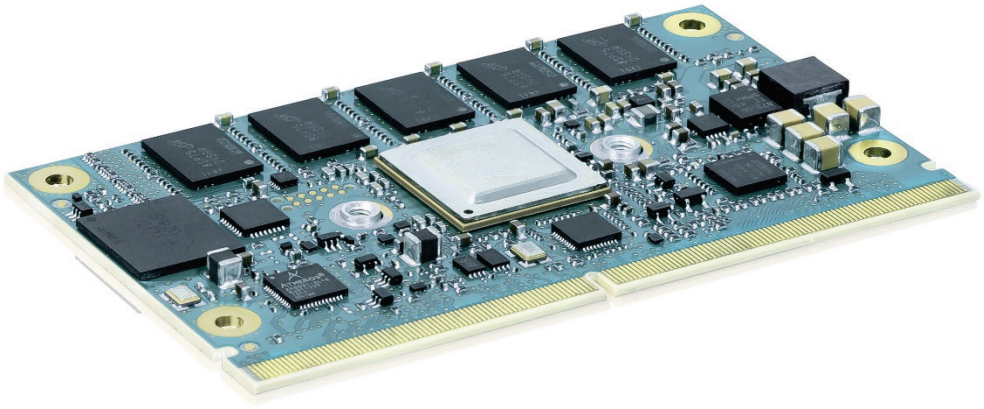
All configuration and setup of the CPU board is either done automatically or manually by the user via the BIOS setup menus.

Latest revision of this manual, datasheet, BIOS, drivers and BSP's (Board Support Packages) can be downloaded from Kontron Web Page.

# 2/ Description

The SMARC-sAL28 is a SMARC half-size module using the NXPs LS1028 processor with dual core ARM. It is designed on the latest SMARC 2.0 specification. The SMARC-sAL28 is a highly integrated, embedded computer board incorporating the edge technology with a dual core SoC from NXP to take advantage of the very optimized power consumption/performance ratio. Due to the integrated Time-Sensitive Networking (TSN) capabilities of the LS1028 and the integrated 4-port Ethernet switch, this board will allow to build very cost effective TSN capable Ethernet gateways for greenfield and brownfield applications.

**Figure 1: Half-size Card with SMARC interface**



## 2.1. SMARC™ Computer-on-Modules

The SMARC™ standard was developed especially for new modules with ARM- and SoC-processors. Boards with this interfaces are characterized by the extremely flat form factor. The SMARC or MXM 3.0 connector comes with 314 pins and a construction height of just 4.3 millimeters. The connector is also available in a shock- and vibration-resistant version for rough environmental conditions.

Furthermore, the standard integrates dedicated interfaces for the latest ARM, x86 and SoC processors like LVDS, 24-bit RGB and HDMI support. OEMs profit from minimized design effort and low Bill of Material (BoM) costs. SMARC™ defines two different module sizes in order to offer a high level of flexibility regarding different mechanical requirements.

Main characteristics of the SMARC-sAL28 are:

- Dual-Core Cortex A-72 on a SMARC short size form factor
- Based on LS1028 from NXP – one SKU with configurable Serialiser/Deserialiser SERDES lines (5 W target TDP)
- Up to 4 GB DDR3L non-ECC and ECC memory down, ECC as default, 8 GbE as option
- One PCIe line can be used as QSGMII port to drive 4x 1 GB TSN capable Ethernet ports
- 3D GPU
- DP support (default)
- LVDS Display support (resistor option)
- Alternative eDP (resistor option)
- 2x Gigabit Ethernet, Wake on LAN (WoL) support, TSN capable
- Support for Audio and common features (SPI, I2C, SMB etc.)
- Chip integrated security solution support
- Full industrial grade temp. range E2 (-40°C up to +85°C) for standard SKUs, commercial version possible
- eMMC flash onboard
- Optional APPROTECT (security chip) support on request, more information under https://www.kontron.de/products/solutions/security/approtect.html

## 2.2. Standard Variants

Following standard variants are available:

**Table 1: Product Numbers of SMARC-sAL28**

| Product Number | Board | Description |
|---|---|---|
| 51011-0208-13-2-2 | SMARC-sAL28, LS1028 dual, 2E/8S, NW 2 | SMARC with NXP LS1028, 1,3 GHz dual core; 2 GB DDR3L ECC, 8 GB eMMC SLC, Networkconfig 2, 2x PCIe, audio, DP, industrial temperature |
| 51011-0408-13-2-3 | SMARC-sAL28, LS1028 dual, 4E/8S, NW 3 | SMARC with NXP LS1028, 1,3 GHz dual core; 4 GB DDR3L ECC, 8 GB eMMC SLC, Networkconfig 3, 2x PCIe, audio, DP, industrial temperature |
| 51011-0432-13-2-4 | SMARC-sAL28, LS1028 dual, 4E/32S, NW 4 | SMARC with NXP LS1028, 1,3 GHz dual core; 4 GB DDR3L ECC, 32 GB eMMC SLC, Networkconfig 4, 2x PCIe, no audio, DP, industrial temperature |

## 2.3. Network Configuration Options

**Table 2: Product Variants of SMARC-sAL28**

| Variant | Description |
|---|---|
| Network Variant 1<br>(Single PHY module, optional) | ▶ Available on customer request<br>▶ SMARC with NXP LS1028, 1.3 GHz dual core; 2 GB DDR3L ECC, 8 GB eMMC SLC, DP, industrial temperature<br>▶ GBE0 PHY connected to RGMII (L0) to CPU (not TSN capable)<br>▶ GBE1 not connected on module, GBE1 could be used on custom carrier to support 2.5 GBE<br>▶ no audio<br>▶ "TSN" variant, although GBE0 is not TSN capable, thus the TSN function needs a TSN carrier.<br>▶ TSN-on-carrier (board provides the 4 TSN capable ports on PCIe D by QSGMII lane)<br>▶ 4 lanes available towards the carrier<br>▶ Possible PCIe options (lane AB/CD), one of<br>▶ 2x PCIe x1<br>▶ 1x PCIe x1 + 1x SATA<br>▶ 1x PCIe x2 + 1x PCIe x1<br>▶ 2x PCIe x2 (no TSN-On-Carrier)<br>▶ 1x PCIe x4, with custom carrier, because special lane order (CDAB instead of ABCD), (no TSN-On-Carrier) |
| Network Variant 2<br>(Dual TSN port module) | ▶ SMARC with NXP LS1028, 1.3 GHz dual core; 2 GB DDR3L ECC, 8 GB eMMC SLC, DP, industrial temperature<br>▶ GBE0 PHY connected to SGMII (L0) to the internal switch<br>▶ GBE1 PHY connected to SGMII (L1) to the internal switch<br>▶ no direct network operation without switch up and running<br>▶ Dual port TSN Endpoint (no need of additional PHYs on Carrier)<br>▶ Audio<br>▶ no QSGMII lane<br>▶ Possible PCIe options (lane A/B), one of<br>▶ 2x PCIe x1 |

| Variant | Description |
|---|---|
| | ▶ 1x PCIe x2<br>▶ 1x PCIe x1 + 1x SATA |
| **Network Variant 3**<br>**(Single PHY module)** | ▶ SMARC with NXP LS1028, 1.3 GHz dual core; 4 GB DDR3L ECC, 8 GB eMMC SLC, DP, industrial temperature<br>▶ GBE0 PHY connected to SGMII (L0) to CPU (TSN capable)<br>▶ GBE1 PHY not connected, GBE1 could be used on custom carrier to support 2.5 GBE<br>▶ 5 ports in total<br>▶ audio<br>▶ TSN-on–Carrier (board provides the 4 TSN capable ports on PCIe D by QSGMII lane)<br>▶ Possible PCIe options (lane A/B), one of<br>▶ 2x PCIe x1<br>▶ 1x PCIe x2<br>▶ 1x PCIe x1 + 1x SATA |
| **Network Variant 4**<br>**(Dual PHY module)** | ▶ SMARC with NXP LS1028, 1.3 GHz dual core; 4 GB DDR3L ECC, 32 GB eMMC SLC, DP, industrial temperature<br>▶ GBE0 PHY connected to SGMII (L0) to CPU (TSN capable)<br>▶ GBE0 PHY could be connected to switch<br>▶ GBE1 connected to RGMII to CPU<br>▶ 6 ports in total<br>▶ no audio<br>▶ TSN-on–Carrier (board provides the 4 TSN capable ports on PCIe D by QSGMII lane)<br>▶ Possible PCIe options (lane A/B), one of<br>▶ 2x PCIe x1<br>▶ 1x PCIe x2<br>▶ 1x PCIe x1 + 1x SATA |

Following accessories are available:

- SMARC 2.0 Evaluation Carrier
- SMARC Starter Kit
- KBOX-A-230-LS, including a SMARC-sAl28 Module and a S1914 Carrier exposing the TSN switch Interfaces

## 2.4. SMARC-sAL28 Feature Set

Table 3: SMARC-sAL28 Feature Set

| SMARC™ Feature specification | SMARC™ Specification Maximum Number Possible | SMARC-sAL28 Feature support | Description |
|---|---|---|---|
| LVDS Display support | 2 | 2 | LVDS option disabled<br>Default option is DP |
| CSI Camera support | 2 | No | |
| USB Interface | 6x USB 2.0<br>with 2x USB 3.0 included | 6x USB 2.0<br>with 1x USB 3.0 included | USB0 without OTG support<br>USB3 with USB 3.0 and OTG support |
| PCIe Interface | 4 | 2 | maximum 2 PCIe controller |
| GbE Interface | 2 | Yes | |
| SDIO Interface | 1 | Yes | |
| SPI Interface | 2 | Yes | Each bus with one chip select at standard modules |
| I2S Interface | 2 | 1 | |
| I2C Interface | 5 | 3 | I2C_PM, I2C_GP, I2C_LCD |
| CAN | 2 | 2 | Second CAN interface as option with abandonment of one I2C interface |

# 3/ System Specifications

## 3.1. Component Main Data

The table below summarizes the features of the motherboard.

**Table 4: Component Main Data**

| SMARC-sAL28 | |
|---|---|
| **Form factor** | Smart Mobility Architecture (SMARC) Hardware with 82 mm x 50 mm, max. thickness 6 mm |
| **Processor** | NXP LS28 Layerscape SoC 1.3 GHz, 488 balls FC-BGA, 17x17 mm, 28 nm CMOS |
| **Memory** | DDR3L memory down. Maximum DDR3L memory size 8 GB.<br>Standard products with 2 GB and 4 GB are available.<br>For cost reductions lower memory sizes are possible. |
| **Boot Flash** | 2 MB to 32 MB SPI NOR flash |
| **Bootloader/BIOS** | U-Boot Bootloader, Flash for Bootloader connected on SPI1(eSPI). |
| **embedded Multimedia Card (eMMC)** | 8 GB pSLC and 32 GB pSLC on standard products<br>option for up to 64GB pSLC |
| **EEPROM** | 24C32, 4k x 8 (32 kbit) |
| **Temperature Monitoring** | Thermal Monitoring Unit (TMU) with +/- 5°C accuracy (CPU internal)<br>Thermal sensor measurement temperature range is 0°C to 125°C. |
| Onboard Controllers | |
| **Ethernet Controller** | 2x 1 GBE PHY Qualcomm AR8031-AL, WOL support<br>1st PHY via SGMII or RGMII BOM option<br>2nd PHY as BOM option via SGMII |
| **Watchdog** | CPU internal watchdog<br>CPLD watchdog for WDT_TIME_OUT# |
| **RTC** | High accuracy (+/-3 ppm)<br>Low power consumption: current consumption typical below 1 µA |
| **USB HUB** | 7 port USB HUB Microchip USB2517I |
| **Display bridge** | Optional: Display Port to LVDS converter PTN3460I |
| **System Management Controller** | CPLD Intel/Altera MAX V 5M570Z |
| **Security** | Optional: APPROTECT Key 1504-03 connected via USB, no SPI connection |
| **Power management** | CPLD controls payload power down state |
| **Operating System Support** | Linux Yocto<br>Buildroot (https://github.com/kontron/buildroot-external-smarc-sal28)<br>other Operating Systems on customer request |
| Interfaces via Smarc I/O | |
| **USB** | USB0, USB1, USB2, USB3, USB4, USB5: USB Standard 2.0<br>USB3: USB Standard 3.1 GEN1 with OTG support |
| **PCIe** | 4x configurable SERDES lines. Line A and B always present. C and D either used for on module LAN PHYs or as SGMII/XGMII on the carrier (resistor BOM options)<br>Up to 2x PCIe controller |
| **Audio** | I2S0 |

| | |
|---|---|
| **Display** | Display port as standard option, FHD (1920x1080) and UHD (3840x2160)<br>Optional: Dual channel LVDS up to 1920x1200 with NXP PTN3460I |
| **SD-Card** | 1x SDIO |
| **UART** | SER0 with RTC/CTS hardware flow control to CPU<br>SER1, SER2 RX/TX |
| **Serial Peripheral Interface (SPI0)** | One chip select available at standard module<br>Optional: second chip select possible with abandonment of USB3 power control from CPU |
| **eSPI/SPI1** | XSPI_A with CS0#, CS1# – CS0# to module SPI-flash (default)<br>Optional: CS0# to edge Connector (for Carrier uboot booting without SPI flash on module)<br>ALERT0#, ALERT1#, SPI_RESET# from CPLD |
| **GPIO** | 12 GPIOs |
| **CAN** | 1x CAN<br>Optional: Second CAN interface with abandonment of one I2C interface |
| Power | |
| **Consumption** | Maximum Power consumption of the board is estimated to 15 W |
| **Input Voltage** | Wide range VCC 3.0 V to 5.25 V<br>vripple_p-p (0-20 MHz) = 200 mV 0.1 – 20 ms input voltage rise ramp to 10% nominal VCC |
| Miscellaneous | |
| **Panel Signal** | Display Port<br>Optional: dual channel LVDS or eDP |
| **Features On Request** | 2x PCIe x2 or 1x PCIe x4 configuration<br>eMMC 5.1 Flash onboard up to 64 GByte pSLC, up to 128 GByte (MLC)<br>Dual Channel LVDS or eDP instead of DP |

## 3.2. Environmental Conditions

**Table 5: Environmental Conditions**

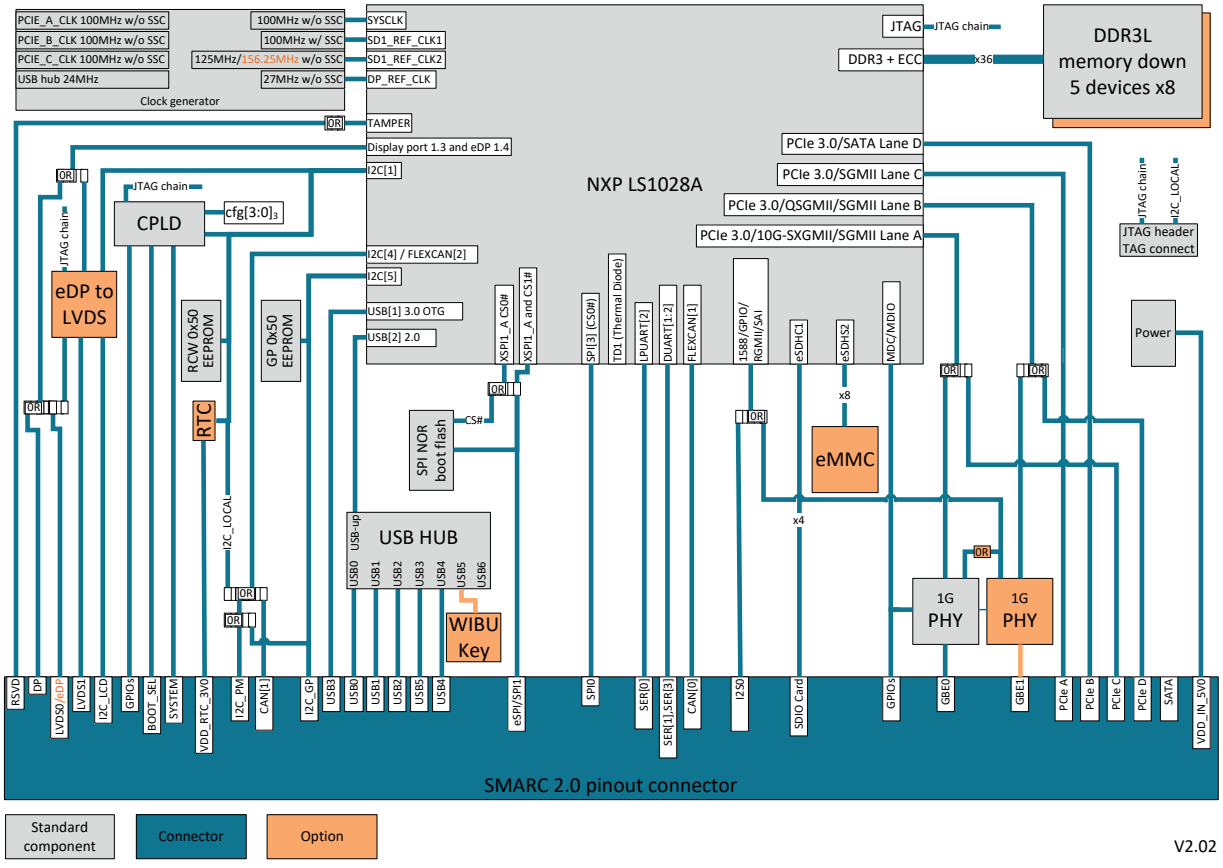
| | |
|---|---|
| **Operating** | ▶ industrial: -40°C to 85°C<br>▶ relative humidity (non-condensing) 10% to 93% at 40°C (acc. to IEC 60068-2-78) |
| **Storage** | ▶ industrial grade: -40°C to +85°C<br>▶ relative humidity (non-condensing) 10 % to 93 % at 40°C (acc. to IEC 60068-2-78) |
| **Electromagnetic Compatibility (EMC)** | according to<br>▶ EN 55032:2015 Electromagnetic compatibility of multimedia equipment - Emission requirements (CISPR 32:2015); German version EN 55032:2015<br>▶ EN 55024:2010 + A1:2015 Information technology equipment - Immunity characteristics - Limits and methods of measurement (CISPR 24:2010 + Cor.:2011 + A1:2015); German version EN 55024:2010 + A1:2015 |
| **CE** | CE according to<br>▶ EN62368-1:2014 + AC:2017<br>▶ EN610000-6-3:2007 + A1:2011<br>▶ CISPR 32: Edition 1.0 2012-01, class B, 1-6 GHz<br>▶ EN55032:2015<br>▶ EN55024:2010 + A1:2015 |
| **UL** | according to IEC 62368-1 (ed.2) |
| **Shock** | ▶ Pulse: half sinus<br>▶ Period: 11 ms<br>▶ Acceleration: 15 g<br>▶ Cycles: three shocks per axis, three axes |

| | |
|---|---|
| **Vibration** | ▶ Sinus from 10 Hz -3000 Hz<br>▶ Amplitude: 10 Hz-57,6 Hz: +/- 0,15 mm<br>▶ Acceleration: 57,6 Hz – 3000Hz: 2 g<br>▶ Cycles: 10 per axis, three axes |
| **Theoretical MTBF** | estimated 10 years at 40°C |
| **RoHS II Compliance** | The product is RoHS II compliant |

## 3.3. Functional Block Diagram

The block diagram shows all available interfaces on the sAL28 module.

**Figure 2: Block Diagram**



# 4/ Board and Connectors

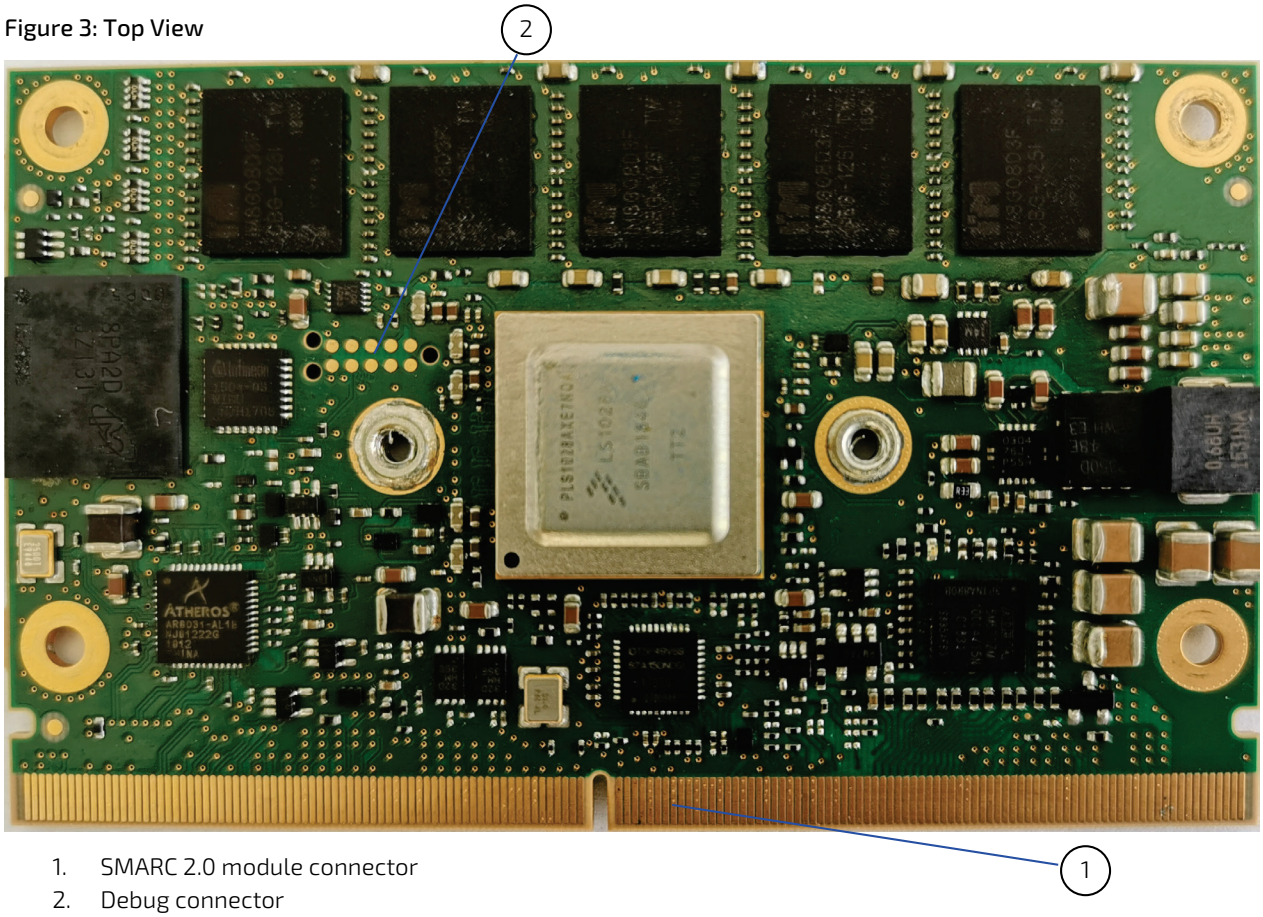
## 4.1.1. Connectors

Table 6: Connectors of SMARC-sAL28

| Connector | Function | Remark |
|---|---|---|
| SMARC | Central Interface | Mating connector: SMARC 2.0 (MXM3) |

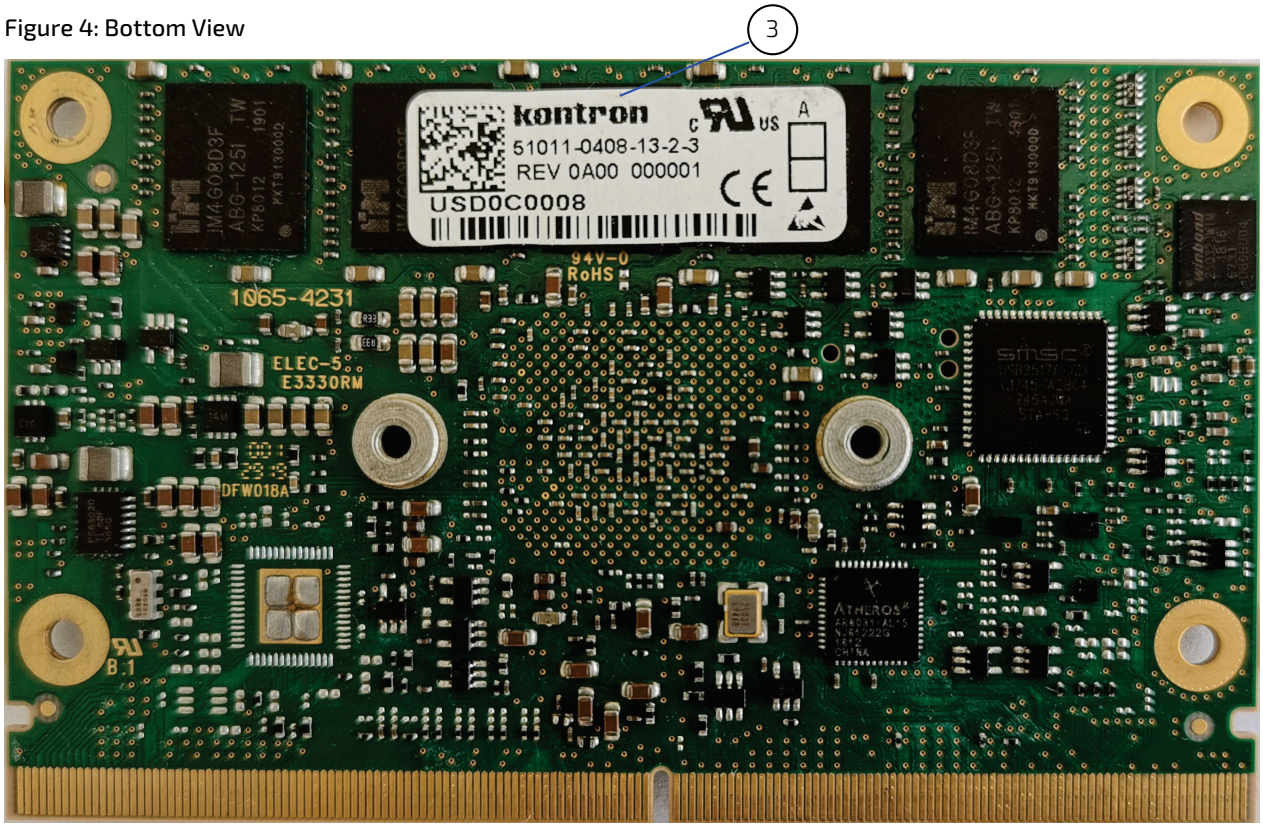
## 4.2. Mainboard view and I/O locations

Figure 3: Top View




1. SMARC 2.0 module connector
2. Debug connector

Figure 4: Bottom View




3. Product label

## 4.3. Mechanical Drawings

Figure 5: Dimensions of SMARC-sAL28

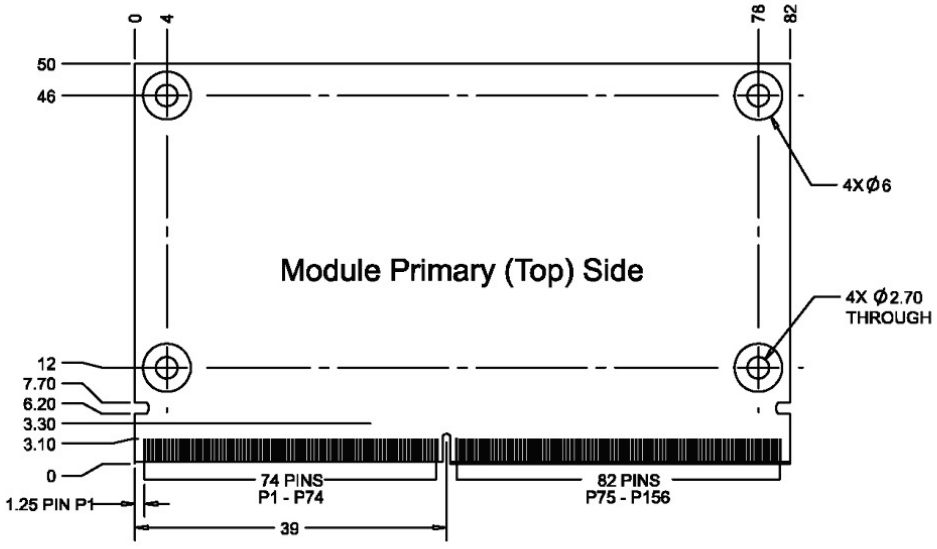
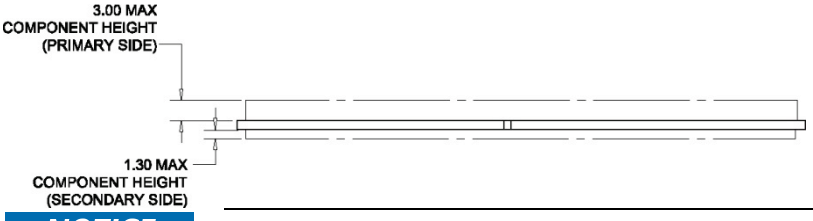



Figure 6: Thickness from side view




**NOTICE** Heat spreader mech. data is available on customer section

# 5/ Pin Definitions

## 5.1. Processor Support

The Dual Cortex A72-Core LS1028A processor is the base for the SMARC 2.0 Computer-on-Module.

**Table 7: Processor Support**

| Name | Speed | RAM. | Cache | TDP/Tj |
|---|---|---|---|---|
| LS1028A | 1.3 GHz | 48 KB L1-I, 32 KB L1-D | 1 MB L2 Cache | 5 W/-40°C to 105°C |

## 5.2. System Memory Support

The memory system has DDR3L memory down with ECC support. Memory size up to 8 GB is possible, options for less size also.

The sAL28 design supports two DDR3L banks with 5 DDR3L devices per bank. Bank 1 is assembled on the top side of the PCB and accessible with chip selects CS0#. The second bank is connected with address mirroring, assembled on the bottom side of the PCB and accessible with chip selects CS1#. Default DDR3L Memory sizes are 2 GByte and 4 GByte.

**Table 8: DDR3L memory options**

| DDR3L memory size | DDR3L memory configuration |
|---|---|
| 512 MB | 5x 1 GBit density 128Mx8 DDR3L parts |
| 1 GByte | 5x 2 GBit density 256Mx8 DDR3L parts |
| 2 GByte | 5x 4 GBit density 512Mx8 DDR3L parts |
| 4 GByte | 10x 4 GBit density 512Mx8 DDR3L parts |
| 8 GByte | 10x 8 GBit density 1024Mx8 DDR3L parts |

## 5.3. SPI NOR Flash

One SPI NOR flash with package WSON8 6x5mm is connected at XSPI1_A interface of LS1028A. Up to 128 GBits (16 Mbytes) are available in this package. Following parts are optional possible:

**Table 9: SPI NOR Flash**

| SPI NOR Flash size | SPI NOR flash configuration |
|---|---|
| 2 Mbytes | 16 MBit serial flash memory with dual SPI |
| 4 Mbytes | 32 MBit serial flash memory with dual SPI |
| 8 Mbytes | 64 MBit serial flash memory with dual SPI |
| 16 Mbytes | 128 MBit serial flash memory with dual SPI |

Default SPI NOR flash part is 4 Mbytes.

## 5.4. I2C Buses

Four I2C buses are available at the SMARC-sAL28 module.

**Table 10: I2C Buses**

| SMARC Connector | I2C Bus | LS1028A | Devices with I2C address |
|---|---|---|---|
| -/- | I2C_LOCAL | IIC1 | DP to LVDS converter PTN3460I (0x20)<br>USB HUB USB2517, (0x2c resistor option)<br>RTC RV8803 (0x32)<br>CPLD (0x4a)<br>RCW EEPROM AT24C32 (0x50) |
| I2C_PM | I2C_PM | IIC4[1] | No devices at module connected |
| I2C_GP | I2C_GP | IIC5 | Module EEPROM AT24C32 (0x50) |
| I2C_LCD | I2C_LCD[2] | -/- | No devices at module connected |

[1] Shares second CAN bus, therefore options to short PM bus with I2C local or I2C GP bus are available

[2] The I2C bus for LCD display (I2C_LCD_SDA, I2C_LCD_SCL) derived from the DP-to-LVDS display converter and is only available with the LVDS display converter option

The SMB_ALERT_1V8# signal derives from CPLD (register 0x1C, bit 1).

## 5.5. SPI Interfaces

Two SPI buses are available at the SMARC-sAL28 module.

**Table 11: SPI Buses**

| SMARC Connector | LS1028A |
|---|---|
| SPI0 | SPI3 |
| ESPI | XSPI1_A |

SPI0 in standard option has one chip select (SPI0_CS0#). Optional the second chip (SPI0_CS1#) select is possible with abandonment of USB3 power control from CPU.

ESPI in standard option has SPI flash on board at the first chip select. The second chip select is available at the SMARC connector (ESPI_CS1#). Optional, the first chip select (ESPI_CS0#) is reconfigurable from SPI flash to the SMARC connector.

The ESPI signals ESPI_ALERT0#, ESPI_ALERT1# and ESPI_RESET# derive from CPLD:
ESPI_ALERT0#: CPLD register 0x1C, bit 2
ESPI_ALERT1#: CPLD register 0x1C, bit 3

## 5.6. eMMC NAND Flash Memory

The SDHC2 interface of the LS1028A is connected to the eMMC.

Specific eMMC Flash memory features are:

- Up to 64 GByte pSLC (or 128 GB MLC)
- eMMC 5.1 specification
- Class 0 (basic); class 2 (block read); class 4 (block write); class 5 (erase); class 6 (write protection); class 7 (lock card)
- HS200 modes
- DDR modes up to 52 MHz clock speed
- ECC and block management

- Boot operation (High-speed boot)
- Sleep mode
- Permanent and power-on write protection
- Replay-protected memory block (RPMB)
- Secure erase and secure trim

**Table 12: eMMC NAND Flash**

| eMMC NAND Flash | Product Number |
|---|---|
| 8 MBytes pSLC | MTFC16GAPALBH-IT |
| 16 MBytes pSLC | MTFC32GAPALBH-IT |
| 32 MBytes pSLC | MTFC64GAPALBH-IT |
| 64 MBytes pSLC | MTFC128GAPALNS-IT |

Pure SLC devices are not available anymore with eMMC technology. The eMMC is reconfigured to pseudo SLC (pSLC) at the standard products. Maximum possible eMMC size with pSLC is 64 Mbytes.

## 5.7. SD-Card Interface

The SDHC1 interface of the LS1028A is connected to the SD-card interface at the Smarc 2.0 connector.

**Table 13: SD-Card Interface**

| SDIO/SDHC Bus | LS1028A | SMARC Connector |
|---|---|---|
| SDIO_D0 | SDHC1_DAT0 | SDIO_D0 |
| SDIO_D1 | SDHC1_DAT1 | SDIO_D1 |
| SDIO_D2 | SDHC1_DAT2 | SDIO_D2 |
| SDIO_D3 | SDHC1_DAT3 | SDIO_D3 |
| SDIO_CK | SDHC1_CLK | SDIO_CK |
| SDIO_CD# | SDHC1_CD# | SDIO_CD# |
| SDIO_CMD | SDHC1_CMD | SDIO_CMD |
| SDIO_WP | SDHC1_WP | SDIO_WP |
| -/- | SDHC1_VSEL[3] | -/- |
| SDIO_PWR_EN | -/-[4] | SDIO_PWR_EN |

[3] Selects between 3.3 V and 1.8 V IO voltage with FET switcher

[4] Controlled from CPLD

## 5.8. SerDes Interfaces

The SerDes Interface in the LS1028A has four lanes. The PCIe and Ethernet interfaces are connected to these four lanes with some restrictions.

The four predefined PCIe SMARC Lane-A to Lane-D are mapped to the SerDes Lanes of the LS1028A in a special order.

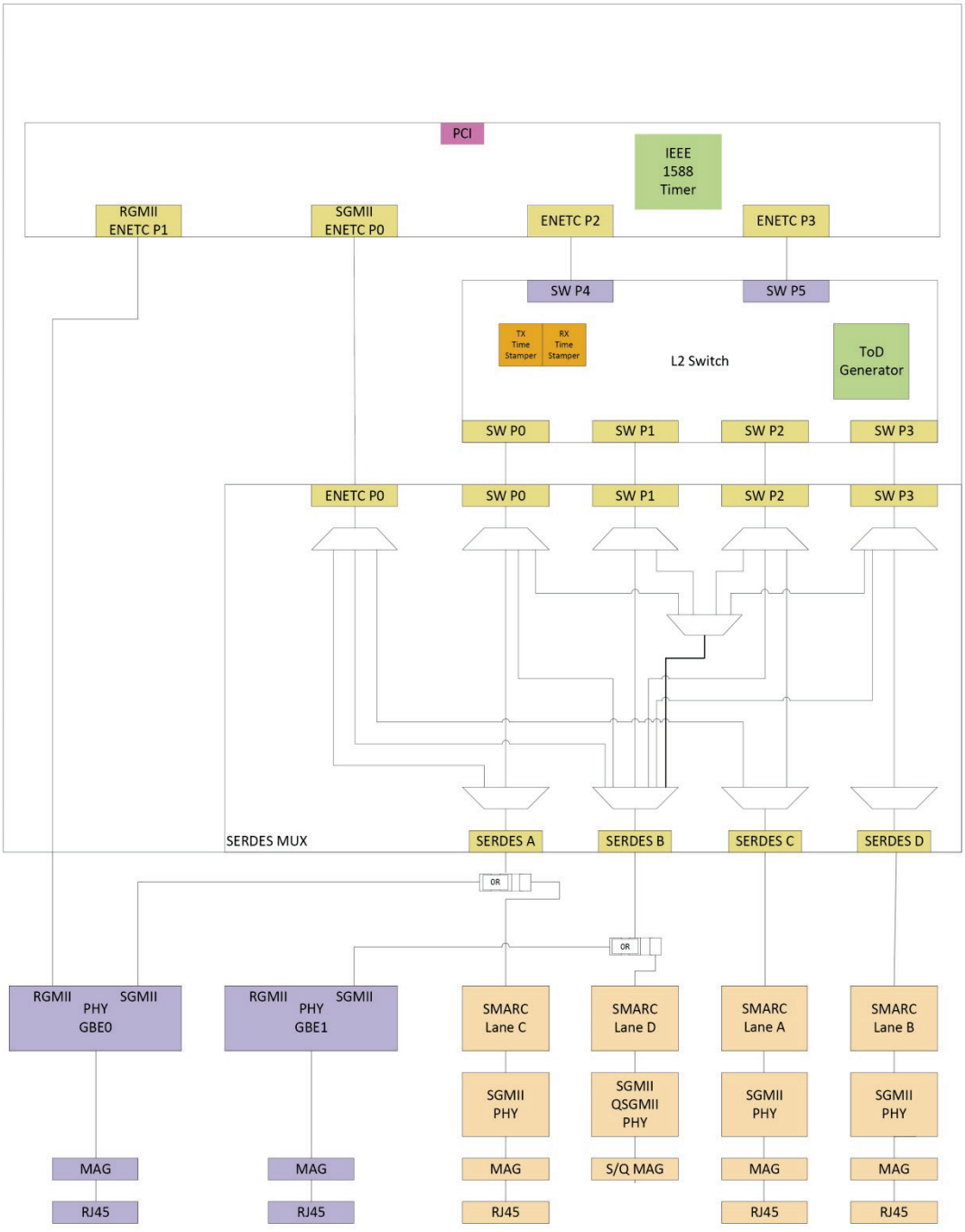
**Table 14: SerDes Interfaces**

| SMARC Connector | LS1028A | Option |
|---|---|---|
| PCIE_A | SD1_TX2/SD1_RX2 (LANE2) | -/- |
| PCIE_B | SD1_TX3/SD1_RX3 (LANE3) | -/- |
| PCIE_C | SD1_TX0/SD1_RX0 (LANE0) | SGMII_L0 (GBE0) |
| PCIE_D | SD1_TX1/SD1_RX1 (LANE1) | SGMII_L1 (GBE1) |

There are maximum 2 PCIe controller and following combinations possible:

- 2x PCIe x1 (PCIe x1: PCIE_A and PCIe x1: PCIE_B)
- 1x PCIe x1 + 1x SATA (PCIe x1: PCIE_A and SATA: PCIE_B)
- 1x PCIe x2 + 1x PCIe x1 (PCIe x2: PCIE_A + PCIE_B x2 and PCIe x1: PCIE_C)
- 2x PCIe x2 (PCIe x2: PCIE_A + PCIE_B and PCIe x2: PCIE_C + PCIE_D)
- 1x PCIe x4, possible with custom carrier, because special lane order (CDAB instead of ABCD)

Figure 7: SerDes Interface Matrix in LS1028A with SMARC PCIe Lanes Connections



## 5.9. CAN Interfaces

There is one CAN interface available with standard boards. A second CAN interface is available if I2C_PM is disabled or shared with I2C_GP or I2C_LOCAL.

**Table 15: CAN Interfaces**

| SMARC Connector | LS1028A | Option |
|---|---|---|
| CAN0 | CAN1 | Available on all standard boards |
| CAN1 | CAN2 | At custom module with restriction for I2C_GP |

## 5.10. USB Interfaces

Six USB 2.0 interfaces are available at the SMARC-sAL28 module. The USB port 3 has also USB 3.1 GEN1 capabilities.

The USB OTG feature is available on port 3, USB port 0 has no OTG feature.

**Table 16: USB Interfaces**

| SMARC Connector | LS1028A | USB HUB USB2517I | Comment |
|---|---|---|---|
| USB0 | -/- | USB HUB port 1 | No OTG feature |
| USB1 | -/- | USB HUB port 2 | |
| USB2 | -/- | USB HUB port 3 | |
| USB3 | USB1 | -/- | With OTG feature<br>with USB 3.1 GEN1 capabilities |
| USB4 | -/- | USB HUB port 4 | |
| USB5 | -/- | USB HUB port 5 | |

### 5.10.1. USB OTG Port

LS1028A USB1 port is used for SMARC USB3 OTG port because this is the only SMARC port which can supports both: OTG and USB 3.1 GEN1.

## 5.11. UART Interfaces

Three UART interfaces are available at the SMARC-sAL28 module.

**Table 17: UART Interfaces**

| SMARC Connector | LS1028A | Comment |
|---|---|---|
| SER0 | LPUART2 | With flow control capabilities (RTS/CTS signals) |
| SER1 | UART1 | Standard serial console for u-boot access<br>No flow control capabilities |
| SER2 | UART2 | No flow control capabilities |
| SER3 | -/- | Not connected on SMARC-sAL28 |

## 5.12. Ethernet Interfaces

Depending on the network configuration, up to two native 1000BaseT Ethernet with AR8031 PHYs (GBE0 and GBE1) are available.

Additional network ports (connected to CPU internal switch) are possible with an external quad port PHY (QSGMII) at the carrier.

There are four possible network variants

**Table 18: Network variants**

| Variant | GBE0 | GBE1 | Comment |
|---|---|---|---|
| 1 | RGMII | -/- | Available on customer request<br>no audio support<br>all PCIe combination possible<br>QSGMII on PCIE_D |
| 2 | SGMII Lane 0 | SGMII LANE 1 | Audio support<br>PCIe on PCIE_A and PCIE_B<br>no QSGMII on PCIE_D |
| 3 | SGMII Lane 0 | -/- | Audio support<br>PCIe on PCIE_A and PCIE_B<br>QSGMII on PCIE_D |
| 4 | SGMII Lane 0 | RGMII | No audio support<br>PCIe on PCIE_A and PCIE_B<br>QSGMII on PCIE_D |

### 5.12.1. GBE0

The GBE0 PHY is available on each network variant.

Network variant 1 has the PHY to CPU connection with RGMII and MDIO address 0x4 (0b00100).

Network variants 2, 3 and 4 has the PHY to CPU connection with SGMII Lane 0 and MDIO address 0x5 (0b00101).

### 5.12.2. GBE1

The GBE1 PHY is available on network variant 2 and 4. Their PHY address in all cases is 0x4 (0b00100).

### 5.12.3. MDIO

There is one MDIO bus for all PHYs - on module PHYs and on carrier PHYs.

PHY addresses on module are 0x4 (0b00100) and 0x5 (0b00101) and cannot be used on carrier.

**Table 19: MDIO Interfaces**

| SMARC Connector | LS1028A | Comment |
|---|---|---|
| MDIO | EMI1_MDIO | 2k21 pull-up to 1.8V on module |
| MDC | EMI1_MDC | Decoupled with 1.8V 74LVD1G17 Schmitt trigger buffer |

### 5.12.4. QSGMII

On network variant 1, 3 and 4 there is one QSGMII interface available at SMARC 2.0 connector port PCIE_D.

With a suitable carrier (e.g. KBOX A-230-LS) this interface allows 4 additional 1000Base-T network ports. These ports connects the CPU with the CPU internal TSN capable switch.

## 5.13. Audio Interfaces

Up to one I2C audio interface is available at the SMARC-sAL28 module.

The network variants 2 and 3 can support the audio feature.

**Table 20: Audio Interface**

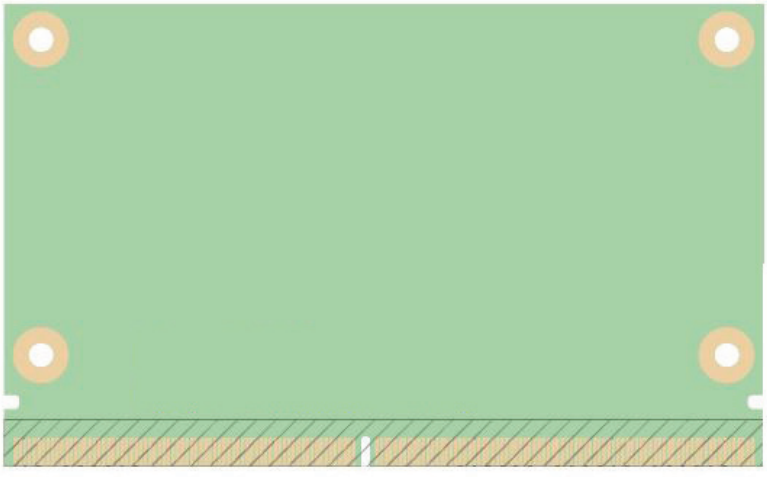
| SMARC Connector | LS1028A | Comment |
|---|---|---|
| AUDIO_MCK | FTM1_CH2 | Whole-numbered divider frequencies of 400MHz possible<br>Default is 1.25MHz |
| I2S0_CK | SAI5_RX_BCLK<br>SAI6_TX_BCLK | |
| I2S0_LRCK | SAI5_RX_SYNC<br>SAI6_TX_SYNC | |
| I2S0_SDIO | SAI5_RX_DATA | |
| I2S0_SDOUT | SAI6_TX_DATA | |

## 5.14. SMARC Connector

The SMARC connector has different pins on both sides:

- Top side: 74 pins are on the left side, 82 pins on the right side
- Bottom side: 75 pins are on the left side, 83 pins on the right side

**Figure 8: 314-pin SMARC Connector,**



## 5.15. Pinout of SMARC sAL28 Connector

### 5.15.1. Pinout of SMARC sAL28 Topside Connector

Table 21: Pinout of SMARC sAL28 Topside Connector

| Pin | Signal | Module Direc-tion | Module Termina-tion | Type/ Tolerance | Connected Device | Device pin name |
|---|---|---|---|---|---|---|
| P1 | SMB_ALERT_1V8# | In | PU-475k | CMOS 1.8V | CPLD | IO_A6 |
| P2 | GND | - | - | GND | GND | GND |
| P3 | CSI1_CK+ | In | - | LVDS D-PHY | - | - |
| P4 | CSI1_CK- | In | - | LVDS D-PHY | - | - |
| P5 | GBE1_SDP | Bi-Dir | PU-10k | CMOS 3.3V | AR8031/LS1028A | PPS/ SWITCH_1588_DAT1 |
| P6 | GBE0_SDP | Bi-Dir | PU-10k | CMOS 3.3V | AR8031/LS1028A | PPS/ SWITCH_1588_DAT0 |
| P7 | CSI1_D0+ | In | - | LVDS D-PHY | - | - |
| P8 | CSI1_D0- | In | - | LVDS D-PHY | - | - |
| P9 | GND | - | - | GND | GND | GND |
| P10 | CSI1_D1+ | In | - | LVDS D-PHY | - | - |
| P11 | CSI1_D1- | In | - | LVDS D-PHY | - | - |
| P12 | GND | - | - | GND | GND | GND |
| P13 | CSI1_D2+ | In | - | LVDS D-PHY | - | - |
| P14 | CSI1_D2- | In | - | LVDS D-PHY | - | - |
| P15 | GND | - | - | GND | GND | GND |
| P16 | CSI1_D3+ | IN | - | LVDS D-PHY | - | - |
| P17 | CSI1_D3- | IN | - | LVDS D-PHY | - | - |
| P18 | GND | - | - | GND | GND | GND |
| P19 | GBE0_MDI3- | Bi-Dir | - | GBE MDI | AR8031 | TRX3- |
| P20 | GBE0_MDI3+ | Bi-Dir | - | GBE MDI | AR8031 | TRX3+ |
| P21 | GBE0_LINK100# | Out/ OD | - | CMOS 3.3V | AR8031 | LED_LINK10_100 |
| P22 | GBE0_LINK1000# | Out/ OD | - | CMOS 3.3V | AR8031 | LED_LINK1000 |
| P23 | GBE0_MDI2- | Bi-Dir | - | GBE MDI | AR8031 | TRX2- |
| P24 | GBE0_MDI2+ | Bi-Dir | - | GBE MDI | AR8031 | TRX2+ |
| P25 | GBE0_LINK_ACT# | Out/ OD | - | CMOS 3.3V | AR8031 | LED_ACT |
| P26 | GBE0_MDI1- | Bi-Dir | - | GBE MDI | AR8031 | TRX1- |
| P27 | GBE0_MDI1+ | Bi-Dir | - | GBE MDI | AR8031 | TRX1+ |
| P28 | GBE0_CTREF | Out | - | - | - | - |
| P29 | GBE0_MDI0- | Bi-Dir | - | GBE MDI | AR8031 | TRX0- |
| P30 | GBE0_MDI0+ | Bi-Dir | - | GBE MDI | AR8031 | TRX0+ |
| P31 | SPI0_CS1# | Out | PU-10k | CMOS 1.8V | LS1028A | SPI3_PCS2 |
| P32 | GND | - | - | GND | GND | GND |
| P33 | SDIO_WP | In | PU-10k | CMOS 3.3V | LS1028A | SDHC1_WP |
| P34 | SDIO_CMD | Bi-Dir | PU-10k | CMOS 3.3V/1.8V | LS1028A | SDHC1_CMD |
| P35 | SDIO_CD# | In | PU-10k | CMOS 3.3V | LS1028A | SDHC1_CD_B |
| P36 | SDIO_CK | Out | Serial-0R | CMOS 3.3V/1.8V | LS1028A | SDHC1_CLK |
| P37 | SDIO_PWR_EN | Out | PU-1k | CMOS 3.3V | CPLD | IO_K7 |
| P38 | GND | - | - | GND | GND | GND |
| P39 | SDIO_D0 | Bi-Dir | - | CMOS 3.3V/1.8V | LS1028A | SDHC1_DAT0 |
| P40 | SDIO_D1 | Bi-Dir | - | CMOS 3.3V/1.8V | LS1028A | SDHC1_DAT1 |

| Pin | Signal | Module Direc-tion | Module Termina-tion | Type/ Tolerance | Connected Device | Device pin name |
|---|---|---|---|---|---|---|
| P41 | SDIO_D2 | Bi-Dir | - | CMOS 3.3V/1.8V | LS1028A | SDHC1_DAT2 |
| P42 | SDIO_D3 | Bi-Dir | - | CMOS 3.3V/1.8V | LS1028A | SDHC1_DAT3 |
| P43 | SPI0_CS0# | Out | PU-4k75 | CMOS 1.8V | LS1028A | SPI3_PCS0 |
| P44 | SPI0_CK | Out | - | CMOS 1.8V | LS1028A | SPI3_SCK |
| P45 | SPI0_DIN | In | - | CMOS 1.8V | LS1028A | SPI3_SIN |
| P46 | SPI0_DO | Out | - | CMOS 1.8V | LS1028A | SPI3_SOUT |
| P47 | GND | - | - | GND | GND | GND |
| P48 | SATA_TX+ | Out | - | SATA | - | - |
| P49 | SATA_TX- | Out | - | SATA | - | - |
| P50 | GND | - | - | GND | GND | GND |
| P51 | SATA_RX+ | In | - | SATA | - | - |
| P52 | SATA_RX- | In | - | SATA | - | - |
| P53 | GND | - | - | GND | GND | GND |
| P54 | ESPI_CS0# | Out | PU-10k | CMOS 1.8V | LS1028A option | XSPI1_A_CS0_B |
| P55 | ESPI_CS1# | Out | PU-10k | CMOS 1.8V | LS1028A | XSPI1_A_CS1_B |
| P56 | ESPI_CK | Out | Serial-33R2 | CMOS 1.8V | LS1028A | XSPI1_A_SCK |
| P57 | ESPI_IO_0 | In | - | CMOS 1.8V | LS1028A | XSPI1_A_DATA0 |
| P58 | ESPI_IO_1 | Out | - | CMOS 1.8V | LS1028A | XSPI1_A_DATA1 |
| P59 | GND | - | - | GND | GND | GND |
| P60 | USB0+ | Bi-Dir | - | USB | USB hub | USB_DN_D1+ |
| P61 | USB0- | Bi-Dir | - | USB | USB hub | USB_DN_D1- |
| P62 | USB0_EN_OC# | Bi-Dir OD | PU-4k75 | CMOS 3.3V | USB hub | PRTPWR1 |
| P63 | USB0_VBUS_DET | In | - | CMOS 3.3V | - | - |
| P64 | USB0_OTG_ID | In | - | CMOS 3.3V | - | - |
| P65 | USB1+ | Bi-Dir | - | USB | USB hub | USB_DN_D2+ |
| P66 | USB1- | Bi-Dir | - | USB | USB hub | USB_DN_D2- |
| P67 | USB1_EN_OC# | Bi-Dir OD | PU-4k75 | CMOS 3.3V | USB hub | PRTPWR2 + OCS2 |
| P68 | GND | - | - | GND | GND | GND |
| P69 | USB2+ | Bi-Dir | - | USB | USB hub | USB_DN_D3+ |
| P70 | USB2- | Bi-Dir | - | USB | USB hub | USB_DN_D3- |
| P71 | USB2_EN_OC# | Bi-Dir OD | PU-4k75 | CMOS 3.3V | USB hub | PRTPWR3 + OCS3 |
| P72 | RSVD | - | 1.8V | PWR | Tamper Power | - |
| P73 | RSVD | - | - | - | - | - |
| P74 | USB3_EN_OC# | Bi-Dir OD | PU-4k75 | CMOS 3.3V | CPLD | IO_G2 |
| P75 | PCIE_A_RST# | Out | PU-CPLD | CMOS 3.3V | CPLD | IO_B1 |
| P76 | USB4_EN_OC# | Bi-Dir OD | PU-4k75 | CMOS 3.3V | USB hub | PRTPWR4 |
| P77 | RSVD | - | - | - | - | - |
| P78 | RSVD | - | - | - | - | - |
| P79 | GND | - | - | GND | GND | GND |
| P80 | PCIE_C_REFCK+ | Out | Serial-33R2 | LVDS PCIe | 5P49V6967 | OUT7+ |
| P81 | PCIE_C_REFCK- | Out | Serial-33R2 | LVDS PCIe | 5P49V6967 | OUT7- |
| P82 | GND | - | - | GND | GND | GND |

| Pin | Signal | Module Direc-tion | Module Termina-tion | Type/ Tolerance | Connected Device | Device pin name |
|---|---|---|---|---|---|---|
| P83 | PCIE_A_REFCK+ | Out | Serial-33R2 | LVDS PCIe | 5P49V6967 | OUT5+ |
| P84 | PCIE_A_REFCK- | Out | Serial-33R2 | LVDS PCIe | 5P49V6967 | OUT5- |
| P85 | GND | - | - | GND | GND | GND |
| P86 | PCIE_A_RX+ | In | - | LVDS PCIe | LS1028A | SD1_RX2_P |
| P87 | PCIE_A_RX- | In | - | LVDS PCIe | LS1028A | SD1_RX2_N |
| P88 | GND | - | - | GND | GND | GND |
| P89 | PCIE_A_TX+ | Out | Seriell-220n | LVDS PCIe | LS1028A | SD1_TX2_P |
| P90 | PCIE_A_TX- | Out | Seriell-220n | LVDS PCIe | LS1028A | SD1_TX2_N |
| P91 | GND | - | - | GND | GND | GND |
| P92 | HDMI_D2+/ DP1_LANE0+ | Out | - | TMDS | - | - |
| P93 | HDMI_D2-/ DP1_LANE0- | Out | - | TMDS | - | - |
| P94 | GND | - | - | GND | GND | GND |
| P95 | HDMI_D1+ / DP1_LANE1+ | Out | - | TMDS | - | - |
| P96 | HDMI_D1-/ DP1_LANE1- | Out | - | TMDS | - | - |
| P97 | GND | - | - | GND | GND | GND |
| P98 | HDMI_D0+/ DP1_LANE2+ | Out | - | TMDS | - | - |
| P99 | HDMI_D0-/ DP1_LANE2- | Out | - | TMDS | - | - |
| P100 | GND | - | - | GND | GND | GND |
| P101 | HDMI_CK+ / DP1_LANE3+ | Out | - | TMDS | - | - |
| P102 | HDMI_CK-/ DP1_LANE3- | Out | - | TMDS | - | - |
| P103 | GND | - | - | GND | GND | GND |
| P104 | HDMI_HPD/ DP1_HPD | In | - | CMOS 1.8V | - | - |
| P105 | HDMI_CTRL_CK/ DP1_AUX+ | Out | - | CMOS 1.8V | - | - |
| P106 | HDMI_CTRL_DAT/ DPS1_AUX- | Bi-Dir | - | CMOS 1.8V | - | - |
| P107 | DP1_AUX_SEL | In | - | CMOS 1.8V | - | - |
| P108 | GPIO0/ CAM0_PWR# | Bi-Dir | PU-475k | CMOS 1.8V | CPLD | IO_J11 |
| P109 | GPIO1/ CAM1_PWR# | Bi-Dir | PU-475k | CMOS 1.8V | CPLD | IO_H11 |
| P110 | GPIO2/ CAM0_RST# | Bi-Dir | PU-475k | CMOS 1.8V | CPLD | IO_F11 |
| P111 | GPIO3/ CAM1_RST# | Bi-Dir | PU-475k | CMOS 1.8V | CPLD | IO_E11 |
| P112 | GPIO4/ HDA_RST# | Bi-Dir | PU-475k | CMOS 1.8V | CPLD | IO_D11 |
| P113 | GPIO5/ PWM_OUT | Bi-Dir | PU-475k | CMOS 1.8V | CPLD | IO_C11 |
| P114 | GPIO6/ TACHIN | Bi-Dir | PU-475k | CMOS 1.8V | CPLD | IO_B11 |
| P115 | GPIO7 | Bi-Dir | PU-475k | CMOS 1.8V | CPLD | IO_A11 |
| P116 | GPIO8 | Bi-Dir | PU-475k | CMOS 1.8V | CPLD | IO_A10 |
| P117 | GPIO9 | Bi-Dir | PU-475k | CMOS 1.8V | CPLD | IO_A9 |
| P118 | GPIO10 | Bi-Dir | PU-475k | CMOS 1.8V | CPLD | IO_A8 |

| Pin | Signal | Module Direc-tion | Module Termina-tion | Type/ Tolerance | Connected Device | Device pin name |
|---|---|---|---|---|---|---|
| P119 | GPIO11 | Bi-Dir | PU-475k | CMOS 1.8V | CPLD | IO_K11 |
| P120 | GND | - | - | GND | GND | GND |
| P121 | I2C_PM_CK | Bi-Dir | PU-2k2 | CMOS 1.8V | LS1028A | IIC1_SCL |
| P122 | I2C_PM_DAT | Bi-Dir | PU-2k2 | CMOS 1.8V | LS1028A | IIC1_SDA |
| P123 | BOOT_SEL0# | In | PU-CPLD | CMOS 1.8V | CPLD | IO_J10 |
| P124 | BOOT_SEL1# | In | PU-CPLD | CMOS 1.8V | CPLD | IO_H10 |
| P125 | BOOT_SEL2# | In | PU-CPLD | CMOS 1.8V | CPLD | IO_H9 |
| P126 | RESET_OUT# | Out -OD | Serial-825R PD-1k | CMOS 1.8V | CPLD | IO_L2 |
| P127 | RESET_IN# | In | PU-10k | CMOS 1.8V | LS1028A | PORESET_B |
| P128 | POWER_BTN# | In | PU-CPLD | CMOS 1.8V | CPLD | IO_G10 |
| P129 | SER0_TX | Out | - | CMOS 1.8V | LS1028A | LPUART2_SOUT |
| P130 | SER0_RX | In | - | CMOS 1.8V | LS1028A | LPUART2_SIN |
| P131 | SER0_RTS# | Out | - | CMOS 1.8V | LS1028A | LPUART2_CTS_B |
| P132 | SER0_CTS# | In | - | CMOS 1.8V | LS1028A | LPUART2_RTS_B |
| P133 | GND | - | - | GND | GND | GND |
| P134 | SER1_TX | Out | - | CMOS 1.8V | LS1028A | UART1_SOUT |
| P135 | SER1_RX | In | - | CMOS 1.8V | LS1028A | UART1_SIN |
| P136 | SER2_TX | Out | - | CMOS 1.8V | LS1028A | UART2_SOUT |
| P137 | SER2_RX | In | - | CMOS 1.8V | LS1028A | UART2_SIN |
| P138 | SER2_RTS# | Out | - | CMOS 1.8V | - | - |
| P139 | SER2_CTS# | In | - | CMOS 1.8V | - | - |
| P140 | SER3_TX | Out | - | CMOS 1.8V | - | - |
| P141 | SER3_RX | In | - | CMOS 1.8V | - | - |
| P142 | GND | - | - | GND | GND | GND |
| P143 | CAN0_TX | Out | - | CMOS 1.8V | LS1028A | CAN1_TX |
| P144 | CAN0_RX | In | - | CMOS 1.8V | LS1028A | CAN1_RX |
| P145 | CAN1_TX | Out | - | CMOS 1.8V | LS1028A option | IIC4_SCL |
| P146 | CAN1_RX | In | - | CMOS 1.8V | LS1028A option | IIC4_SDA |
| P147 | VDD_IN | PWR | - | 3.0V - 5.25V | Power | - |
| P148 | VDD_IN | PWR | - | 3.0V - 5.25V | Power | - |
| P149 | VDD_IN | PWR | - | 3.0V - 5.25V | Power | - |
| P150 | VDD_IN | PWR | - | 3.0V - 5.25V | Power | - |
| P151 | VDD_IN | PWR | - | 3.0V - 5.25V | Power | - |
| P152 | VDD_IN | PWR | - | 3.0V - 5.25V | Power | - |
| P153 | VDD_IN | PWR | - | 3.0V - 5.25V | Power | - |
| P154 | VDD_IN | PWR | - | 3.0V - 5.25V | Power | - |
| P155 | VDD_IN | PWR | - | 3.0V - 5.25V | Power | - |
| P156 | VDD_IN | PWR | - | 3.0V - 5.25V | Power | - |

## 5.15.2. Pinout of SMARC sAL28 Bottom Side Connector

Table 22: Pinout of SMARC sAL28 Bottom Side Connector

| Pin | Signal | Module Direc-tion | Module Termina-tion | Type/ Tolerance | Connected Device | Device pin name |
|---|---|---|---|---|---|---|
| S1 | CSI1_TX+/ I2C_CAM1_CK | In | - | TMDS/ CMOS 1.8V | - | - |
| S2 | CSI1_TX-/ I2C_CAM1_DAT | In | - | TMDS/ CMOS 1.8V | - | - |
| S3 | GND | - | - | GND | GND | GND |
| S4 | RSVD | - | - | CMOS 1.0V | LS1028A | TA_BB_TMP_DETECT# |
| S5 | CSI0_TX+/ I2C_CAM0_CK | Out | - | CMOS 1.8V - | - | - |
| S6 | CAM_MCK | Out | - | CMOS 1.8V | - | - |
| S7 | CSI0_TX-/ I2C_CAM0_DAT | Bi-Dir | - | CMOS 1.8V | - | - |
| S8 | CSI0_CK+ | In | - | LVDS D-PHY | - | - |
| S9 | CSI0_CK- | In | - | LVDS D-PHY | - | - |
| S10 | GND | - | - | GND | GND | GND |
| S11 | CSI0_RX0+ | In | - | LVDS D-PHY | - | - |
| S12 | CSI0_RX0- | In | - | LVDS D-PHY | - | - |
| S13 | GND | - | - | GND | GND | GND |
| S14 | CSI0_RX1+ | In | - | LVDS D-PHY | - | - |
| S15 | CSI0_RX1- | In | - | LVDS D-PHY | - | - |
| S16 | GND | - | - | GND | GND | GND |
| S17 | GBE1_MDI0+ | Bi-Dir | - | GBE MDI | AR8031 | TRX0+ |
| S18 | GBE1_MDI0- | Bi-Dir | - | GBE MDI | AR8031 | TRX0- |
| S19 | GBE1_LINK100# | Out/ OD | - | CMOS 3.3V | AR8031 | LED_LINK10_100 |
| S20 | GBE1_MDI1+ | Bi-Dir | - | GBE MDI | AR8031 | TRX1+ |
| S21 | GBE1_MDI1- | Bi-Dir | - | GBE MDI | AR8031 | TRX1- |
| S22 | GBE1_LINK1000# | Out/ OD | - | CMOS 3.3V | AR8031 | LED_LINK1000 |
| S23 | GBE1_MDI2+ | Bi-Dir | - | GBE MDI | AR8031 | TRX2+ |
| S24 | GBE1_MDI2- | Bi-Dir | - | GBE MDI | AR8031 | TRX2- |
| S25 | GND | Bi-Dir | - | GND | GND | GND |
| S26 | GBE1_MDI3+ | Out | - | GBE MDI | AR8031 | TRX3+ |
| S27 | GBE1_MDI3- | Bi-Dir | - | GBE MDI | AR8031 | TRX3- |
| S28 | GBE1_CTREF | Bi-Dir | - | GBE MDI | - | - |
| S29 | PCIE_D_TX+ | Bi-Dir | Seriell-220n | LVDS PCIe | LS1028A | SD1_TX0+ |
| S30 | PCIE_D_TX- | Bi-Dir | Seriell-220n | LVDS PCIe | LS1028A | SD1_TX0- |
| S31 | GBE1_LINK_ACT# | Out/ OD | - | CMOS 3.3V | AR8031 | LED_ACT |
| S32 | PCIE_D_RX+ | Bi-Dir | Serial-0R | LVDS PCIe | LS1028A | SD1_RX0+ |
| S33 | PCIE_D_RX- | Bi-Dir | Serial-0R | LVDS PCIe | LS1028A | SD1_RX0- |
| S34 | GND | - | - | GND | GND | GND |
| S35 | USB4+ | Bi-Dir | - | USB | USB hub | USB_DN_D4+ |
| S36 | USB4- | Bi-Dir | - | USB | USB hub | USB_DN_D4- |
| S37 | USB3_VBUS_DET | In | - | CMOS 3.3V | LS1028A | USB1_VBUS |
| S38 | AUDIO_MCK | Out | Serial-240R | CMOS 1.8V | LS1028A option | FTM1_CH3 |

| Pin | Signal | Module Direc-tion | Module Termina-tion | Type/ Tolerance | Connected Device | Device pin name |
|---|---|---|---|---|---|---|
| S39 | I2S0_LRCK | Bi-Dir | Serial-0R | CMOS 1.8V | LS1028A option | SAI4_TX_SYNC |
| S40 | I2S0_SDOUT | Out | Serial-0R | CMOS 1.8V | LS1028A option | SAI4_TX_DATA |
| S41 | I2S0_SDIN | In | Serial-oR | CMOS 1.8V | LS1028A option | SAI4_TX_DATA |
| S42 | I2S0_CK | Bi-Dir | Serial-0R | CMOS 1.8V | LS1028A option | SAI4_TX_BCLK |
| S43 | ESPI_ALERT0# | In | PU-CPLD | CMOS 1.8V | CPLD | IO_C6 |
| S44 | ESPI_ALERT1# | In | PU-CPLD | CMOS 1.8V | CPLD | IO_B6 |
| S45 | MDC | OUT | - | CMOS 1.8V | LS1028A option | EMI1_MDC |
| S46 | MDIO | Bi-Dir | PU-2k21 | CMOS 1.8V | LS1028A option | EMI1_MDIO |
| S47 | GND | - | - | GND | GND | GND |
| S48 | I2C_GP_CK | Out | PU-2k21 | CMOS 1.8V | LS1028A | IIC5_SCL |
| S49 | I2C_GP_DAT | Bi-Dir | PU-2k21 | CMOS 1.8V | LS1028A | IIC5_SDA |
| S50 | HDSA_SYNC/ I2S2_LRCK | Bi-Dir | - | CMOS 1.5V/ 1.8V | - | - |
| S51 | HDA_SDO/ I2S2_SDOUT | Out | - | CMOS 1.5V/ 1.8V | - | - |
| S52 | HDA_SDI/ I2S2_SDIN | In | - | CMOS 1.5V/ 1.8V | - | - |
| S53 | HDA_CK/ I2S2_CK | Bi-Dir | - | CMOS 1.5V/ 1.8V | - | - |
| S54 | SATA_ACT# | - | - | CMOS 3.3V | - | - |
| S55 | USB5_EN_OC# | Bi-Dir OD | PU-10k | CMOS 3.3V | USB hub | PRTPWR5 + OCS5# |
| S56 | ESPI_IO_2 | Bi-Dir | - | CMOS 1.8V | LS1028A | XSPI1_A_DATA2 |
| S57 | ESPI_IO_3 | Bi-Dir | - | CMOS 1.8V | LS1028A | XSPI1_A_DATA3 |
| S58 | ESPI_RESET# | Out | - | CMOS 1.8V | CPLD | IO_L5 |
| S59 | USB5+ | Bi-Dir | - | USB | USB hub | USB_DN_D5+ |
| S60 | USB5- | Bi-Dir | - | USB | USB hub | USB_DN_D5- |
| S61 | GND | - | - | GND | GND | GND |
| S62 | USB3_SSTX+ | Bi-Dir | Serial-100n | LVDS_AFB | LS1028A | USB1_TX_P |
| S63 | USB3_SSTX- | Bi-Dir | Serial-100n | LVDS_AFB | LS1028A | USB1_TX_M |
| S64 | GND | - | - | GND | GND | GND |
| S65 | USB3_SSRX+ | Bi-Dir | - | LVDS_AFB | LS1028A | USB1_RX_P |
| S66 | USB3_SSRX- | Bi-Dir | - | LVDS_AFB | LS1028A | USB1_RX_M |
| S67 | GND | - | - | GND | GND | GND |
| S68 | USB3+ | Bi-Dir | - | LVDS_AFB | LS1028A | USB1_D_P |
| S69 | USB3- | Bi-Dir | - | LVDS_AFB | LS1028A | USB1_D_M |
| S70 | GND | - | - | GND | GND | GND |
| S71 | USB2_SSTX+ | Bi-Dir | - | LVDS_AFB | - | - |
| S72 | USB2_SSTX- | Bi-Dir | - | LVDS_AFB | - | - |
| S73 | GND | - | - | GND | GND | GND |
| S74 | USB2_SSRX+ | Bi-Dir | - | LVDS_AFB | - | - |
| S75 | USB2_SSRX- | Bi-Dir | - | LVDS_AFB | - | - |
| S76 | PCIE_B_RST# | Out | PU-CPLD | CMOS 3.3V | CPLD | IO_K8 |
| S77 | PCIE_C_RST# | Out | PU-CPLD | CMOS 3.3V | CPLD | IO_L9 |
| S78 | PCIE_C_RX+ | In | Serial-0R | LVDS PCIe | LS1028A option | SD1_RX1_P |
| S79 | PCIE_C_RX- | In | Serial-0R | LVDS PCIe | LS1028A option | SD1_RX1_N |
| S80 | GND | - | - | GND | GND | GND |
| S81 | PCIE_C_TX+ | Out | Seriell-220n | LVDS PCIe | LS1028A option | SD1_RX1_P |

| Pin | Signal | Module Direc-tion | Module Termina-tion | Type/ Tolerance | Connected Device | Device pin name |
|---|---|---|---|---|---|---|
| S82 | PCIE_C_TX- | Out | Seriell-220n | LVDS PCIe | LS1028A option | SD1_RX1_N |
| S83 | GND | - | - | GND | GND | GND |
| S84 | PCIE_B_REFCK+ | Out | Serial-33R2 | LVDS PCIe | 5P49V6967 | OUT6+ |
| S85 | PCIE_B_REFCK- | Out | Serial-33R2 | LVDS PCIe | 5P49V6967 | OUT6- |
| S86 | GND | - | - | GND | GND | GND |
| S87 | PCIE_B_RX+ | In | - | LVDS PCIe | LS1028A | SD1_RX3_P |
| S88 | PCIE_B_RX- | In | - | LVDS PCIe | LS1028A | SD1_RX3_N |
| S89 | GND | - | - | GND | GND | GND |
| S90 | PCIE_B_TX+ | Out | Seriell-220n | LVDS PCIe | LS1028A | SD1_TX3_P |
| S91 | PCIE_B_TX- | Out | Seriell-220n | LVDS PCIe | LS1028A | SD1_TX3_N |
| S92 | GND | - | - | GND | GND | GND |
| S93 | DP0_LANE0+ | Out | - | LVDS LCD | - | - |
| S94 | DP0_LANE0- | Out | - | LVDS LCD | - | - |
| S95 | DP0_AUX_SEL | In | - | CMOS 1.8V | - | - |
| S96 | DP0_LANE1+ | Out | - | LVDS LCD | - | - |
| S97 | DP0_LANE1- | Out | - | LVDS LCD | - | - |
| S98 | DP0_HPD | In | - | CMOS 1.8V | - | - |
| S99 | DP0_LANE2+ | Out | - | LVDS LCD | - | - |
| S100 | DP0_LANE2- | Out | - | LVDS LCD | - | - |
| S101 | GND | - | - | GND | GND | GND |
| S102 | DP0_LANE3+ | Out | - | LVDS LCD | - | - |
| S103 | DP0_LANE3- | Out | - | LVDS LCD | - | - |
| S104 | USB3_OTG_ID | Out | - | CMOS 3.3V | LS1028A | USB1_ID |
| S105 | DP0_AUX+ | Out | - | LVDS LCD | - | - |
| S106 | DP0_AUX- | Out | - | LVDS LCD | - | - |
| S107 | LCD1_BKLT_EN | Out | - | CMOS 1.8V | - | - |
| S108 | LVDS1_CK+/ eDP1_AUX+/ DSI1_CLK+ | Out | - | LVDS LCD | PTN3460I | LVSCKE_P |
| S109 | LVDS1_CK-/ eDP1_AUX-/ DSI1_CLK- | Out | - | LVDS LCD | PTN3460I | LVSCKE_N |
| S110 | GND | - | - | GND | GND | GND |
| S111 | LVDS1_0+/ EDP1_TX0+/ DSI1_D0+ | Out | - | LVDS LCD | PTN3460I | LVSAE_P |
| S112 | LVDS1_0-/ EDP1_TX0-/ DSI1_D0- | Out | - | LVDS LCD | PTN3460I | LVSAE_N |
| S113 | eDP1_HPD | Out | - | CMOS 1.8V | - | - |
| S114 | LVDS1_1+/ EDP1_TX1+/ DSI1_D1+ | Out | - | LVDS LCD | PTN3460I | LVSBE_P |
| S115 | LVDS1_1-/ EDP1_TX1-/ DSI1_D1- | Out | - | LVDS LCD | PTN3460I | LVSBE_N |
| S116 | LCD1_VDD_EN | Out | - | CMOS 1.8V | - | - |

| Pin | Signal | Module Direc-tion | Module Termina-tion | Type/ Tolerance | Connected Device | Device pin name |
|---|---|---|---|---|---|---|
| S117 | LVDS1_2+/ eDP1_TX2+/ DSI1_D2+ | Out | - | LVDS LCD | PTN3460I | LVSCE_P |
| S118 | LVDS1_2-/ eDP1_TX2-/ DSI1_D2- | Out | - | LVDS LCD | PTN3460I | LVSCE_N |
| S119 | GND | - | - | GND | GND | GND |
| S120 | LVDS1_3+/ eDP1_TX3+/ DSI1_D3+ | Out | - | LVDS LCD | PTN3460I | LVSDE_P |
| S121 | LVDS1_3-/ eDP1_TX3-/ DSI1_D3- | Out | - | LVDS LCD | PTN3460I | LVSDE_N |
| S122 | LCD1_BKLT_PWM | Out | | CMOS 1.8V | - | - |
| S123 | RSVD | Out | - | CMOS 1.8V | LS1028A option | TA_TMP_DETECT# |
| S124 | GND | - | - | GND | GND | GND |
| S125 | LVDS0_0+/ eDP0_TX0+/ DSI0_D0+ | Out | Serial-0R | LVDS LCD | PTN3460I/ LS1028A | LVSAO_P/ DP_LANE0+ |
| S126 | LVDS0_0-/ eDP0_TX0-/ DSI0_D0- | Out | Serial-0R | LVDS LCD | PTN3460I/ LS1028A | LVSAO_N/ DP_LANE0- |
| S127 | LCD0_BKLT_EN | Out | Serial-825R PD-1k | CMOS 1.8V | PTN3456I/CPLD | BKLTEN/ IO_C1 |
| S128 | LVDS0_1+/ eDP0_TX1+/ DSI0_D1+ | Out | Serial-0R | LVDS LCD | PTN3460I/ LS1028A | LVSBO_P/ DP_LANE1+ |
| S129 | LVDS0_1-/ eDP0_TX1-/ DSI0_D1- | Out | Serial-0R | LVDS LCD | PTN3460I/ LS1028A | LVSBO_N/ DP_LANE1- |
| S130 | GND | - | - | GND | GND | GND |
| S131 | LVDS0_2+/ eDP0_TX2+/ DSI0_D2+ | Out | Serial-0R | LVDS LCD | PTN3460I/ LS1028A | LVSCO_P/ DP_LANE2+ |
| S132 | LVDS0_2-/ eDP0_TX2-/ DSI0_D2- | Out | Serial-0R | LVDS LCD | PTN3460I/ LS1028A | LVSCO_N/ DP_LANE2- |
| S133 | LCD0_VDD_EN | Out | Serial-825R PD-1k | CMOS 1.8V | PTN3456I/CPLD | PVCCEN/ IO_H1 |
| S134 | LVDS0_CK+/ eDP0_AUX+/ DSI0_CLK+ | Out | Serial-0R/ Serial-100n PU-100k | LVDS LCD | PTN3460I/ LS1028A | LVSDO_P/ DP_LANE3+ |
| S135 | LVDS0_CK-/ eDP0_AUX-/ DSI0_CLK- | Out | Serial-0R/ Serial-100n PD-100k | LVDS LCD | PTN3460I/ LS1028A | LVSDO_N/ DP_LANE3- |
| S136 | GND | - | - | GND | GND | GND |
| S137 | LVDS0_3+/ eDP0_TX3+/ DSI0_D3+ | Out | Serial-0R | LVDS LCD | PTN3460I/ LS1028A | LVSCKO_P/ DP_AUX+ |
| S138 | LVDS0_3-/ eDP0_TX3-/ DSI0_D3- | Out | Serial-0R | LVDS LCD | PTN3460I/ LS1028A | LVSCKO_N/ DP_AUX- |
| S139 | I2C_LCD_CK | Out | PU-2k21 | CMOS 1.8V | PTN3456I | DDC_SCL |

| Pin | Signal | Module Direc-tion | Module Termina-tion | Type/ Tolerance | Connected Device | Device pin name |
|---|---|---|---|---|---|---|
| S140 | I2C_LCD_DAT | Bi-Dir | PU-2k21 | CMOS 1.8V | PTN3456I | DDC_SDA |
| S141 | LCD0_BKLT_PWM | Out | Serial-825R PD-1k | CMOS 1.8V | PTN3460I/CPLD | PWM0/ IO_L11 |
| S142 | RSVD | - | - | 0.97V - 1.05V | Tamper Power | - |
| S143 | GND | - | - | GND | GND | GND |
| S144 | EDP0_HPD | - | - | CMOS 1.8V | PTN3460I/ LS1028A | HPDRX/ DP_HPD |
| S145 | WDT_TIME_OUT# | Out | - | CMOS 1.8V | CPLD | IO_D10 |
| S146 | PCIE_WAKE # | In | PU-4k75 | CMOS 3.3V | CPLD | IO_F2 |
| S147 | VDD_RTC | - | Serial-1k | PWR | RTC | power |
| S148 | LID# | In | PU-4k75 | CMOS 1.8V | CPLD | IO_D9 |
| S149 | SLEEP# | In | PU-4k75 | CMOS 1.8V | CPLD | IO_B10 |
| S150 | VIN_PWR_BAD# | In | PU-10k | CMOS VDDIN | power circuit | - |
| S151 | CHARGING# | In | PU-CPLD | CMOS 1.8V | CPLD | IO_C10 |
| S152 | CHARGER_PRSNT# | In | PU-CPLD | CMOS 1.8V | CPLD | IO_F10 |
| S153 | CARRIER_STBY# | Out | Serial-825R PD-1k | CMOS 1.8V | CPLD | IO_L6 |
| S154 | CARRIER_PWR_ ON | Out | - | CMOS 1.8V | power circuit | - |
| S155 | FORCE_RECOV# | In | PU-4k75 | CMOS 1.8V | CPLD | IO_B2 |
| S156 | BATLOW# | In | PU_CPLD | CMOS 1.8V | CPLD | IO_G11 |
| S157 | TEST# | In | PU-10k | CMOS 1.8V | CPLD | IO_B2 |
| S158 | GND | - | - | GND | GND | GND |

## 5.16. JTAG Debug connector

**Table 23: JTAG Debug connector**

| Pin# | Signal | Description |
|---|---|---|
| 1 | JTAG_TCK | JTAG clock |
| 2 | JTAG_TMS | JTAG test mode select |
| 3 | PORESET# | Power on reset for LS1028A, low active signal [3] |
| 4 | JTAG_TDO | JTAG test data output |
| 5 | V_3V3_S0 | 3.3V supply and I/O level voltage use also for JTAG_EN_3V3 |
| 6 | JTAG_TDI | JTAG test data input |
| 7 | JTAG_EN_3V3 | JTAG enable, high active signal |
| 8 | I2C_LOCAL_SDA_3V3 | I2C_LOCAL bus data signal, I/O level: 3.3V |
| 9 | GND | Ground |
| 10 | I2C_LOCAL_SCL_3V3 | I2C_LOCAL bus clock signal, I/O level: 3.3V |

[3] need to be an open drain signal (push/pull with direct connection of CodeWarrior TAP would not work)

# 6/ Configuration

## 6.1. Boot Mode

The following table shows the possible boot sources on the carrier board defined in SMARC 2.0 spec:

**Table 24: Boot Options on the carrier board**

| | Carrier Connection | | | Boot Source | Supported on sAL28 |
|---|---|---|---|---|---|
| | BOOT_SEL2# | BOOT_SEL1# | BOOT_SEL0# | | |
| 0 | GND | GND | GND | Carrier SATA | No |
| 1 | GND | GND | Float | Carrier SD Card | From U-Boot |
| 2 | GND | Float | GND | Carrier eSPI (CS0#) | From U-Boot |
| 3 | GND | Float | Float | Carrier SPI (CS0#) | From U-Boot |
| 4 | Float | GND | GND | Module device (NAND, NOR) | No |
| 5 | Float | GND | Float | Remote boot (GBE, serial) | From U-Boot |
| 6 | Float | Float | GND | Module eMMC Flash | From u-boot |
| 7 | Float | Float | Float | Module SPI | From u-boot |

When the CPLD code is active, the SL1028A boot selection pins are pulled from CPLD to boot from I2C_LOCAL bus (LS1028A I2C1). The EEPROM at I2C_LOCAL bus (address 0x50) contains RCW and PBI which selects the XSPI1_A bus with chip select 0 to boot from the connected SPI NOR flash.

If the CPLD is not active or if the boot process did not work from I2C1 the SL1028A boot selection pins can be pulled to XSPI1_A bus which is the default failsafe mechanism in CPLD.

Boot from external SPI is possible with resistor option: disconnect SL1028A chip select 0 from SPI flash and connect SL1028A chip select 0 with SMARC connector ESPI_CS0.

## 6.2. Configurable Watchdog

There are two watchdogs: a CPU internal and CPLD support watchdog.

## 6.3. RTC current consumption

The VDD_RTC pin at the SMARC 2.0 Connector has the ability to charge a gold cap capacitor on the carrier. The power source of the VDD_RTC voltage is V_3V3_S5 with BAS70 as series protection diode and an additional series resistance of 240 Ohm.

Optionally, the series resistance is replaceable with an additional BAS70 diode to protect a battery circuit on a carrier which has no diode protection (disable gold cap charging capability).

**Table 25: Maximum current consumption of RTC**

| Ambient temperature | Maximum Current in VDD_RTC |
|---|---|
| -20°C | 0.4 µA |
| 25°C | 0.6 µA |
| 85°C | 1.8 µA |

## 6.4. Power Control

### 6.4.1. Power Supply

The SMARC-sAL28 supports a power input from 3.0 to 5.25V. The supply voltage is applied through the VCC pins (VCC) of the module connector. Considered current rating of protective device is part of End-Equipment.

The following parameters should be delivered from the carrier board:

- Voltage Ripple maximum 100 mV peak to peak 0-20 MHz to 20 ms rise time from input voltage <10% to nominal VCC
- Max allowed inrush current: connector limit (15 W @ 3,0 V)
- There are 5x 47u 1210 10 V bulk capacitors too meet the required noise and ripple requirements.

Table 26: Power Supply Specifications

| Voltage rail | Required range | Controller | Frequency |
|---|---|---|---|
| V_5V0_IN | 3.0V – 5.25V | Input power | -/- |
| V_3V3_S5 | 3.15V – 3.45V | Buck-Boost | 2.4 MHz PFM |
| V_1V8_S5 | 1.71V – 1.89V | LDO | -/- |
| V_3V3_S0 | 3.15V – 3.45V | Switch TPS22964 | -/- |
| V_1V8_S0 | 1.7V – 1.9V | Buck TLV62084A | 2 MHz PWM/PFM |
| V_1V35_S0 | 1.283V – 1.45V | Buck TLV62084A | 2 MHz PWM/PFM |
| V_1V0_S0 | 0.97V – 1.03V | Buck TLV62084A | 600 kHz PWM |
| V_1V0_SVDD_S0 | 0.971V – 1.05V | Buck TLV62084A | 2 MHz PWM/PFM |
| V_0V675_VTT | 0.6415V – 0.725V | LDO | -/- |

### 6.4.2. Power Button (POWER_BTN#)

The power button (Pin P128) is available through the module connector described in the pinout list. To start the module via Power Button the PWRBTN# signal must be at least 50 ms (50 ms ≤ t < 4 s, typical 400 ms) at low level (Power Button Event).

Pressing the power button for at least 4 seconds will turn off power to the module (Power Button Override).

The module starts automatically after power up to the payload state S0. There is one bit in the NVM where this automatism can be changed: with changed bit the module will stay in state S5 until a power up event occurred. This could be one of this events:

- Power button pressed
- One of the wake lines WOL_INT_GBE#, PCIE_WAKE# or RTC_INT# are asserted

### 6.4.3. Power Management Signals

Following management signals are implemented:

- VIN_PWR_BAD#: Power bad indication from Carrier board. The Module power supply will not be enabled while this signal is held low by the Carrier. VIN_PWR_BAD# is pulled up on Module. VIN_PWR_BAD# is the enable signal for the 3.3V buck-boost converter on the module (first POL converter).

- CARRIER_STBY#: The Module will drive CARRIER_STBY# low by CPLD when the system is in a standby power state.
- CARRIER_PWR_ON: The “last” power good signal in daisy chained POLs configuration controls the CARRIER_PWR_ON signal
- RESET_OUT#: The same “last” power good signal as used for CARRIER_PWR_ON triggers the minimum 100ms delay of the RESET_OUT# in the CPLD. Therefore the RESET_OUT# release arrives between 100ms and 200ms after the CARRIER_PWR_ON release.

### 6.4.4. Battery Control Signals

SLEEP#, BATLOW#, LID#, CHARGING# and CHARGER_PRSNT# are connected to the CPLD and accessible through CPLD GPI register 0x1B:

- SLEEP#: CPLD register 0x1B bit 2
- BATLOW#: CPLD register 0x1B bit 3
- LID#: CPLD register 0x1B bit 4
- CHARGING#: CPLD register 0x1B bit 5
- CHARGER_PRSNT#: CPLD register 0x1B bit 6

**NOTICE**

**If any of the supply voltages drops below the allowed operating level longer than the specified hold-up time, all the supply voltages should be shut down and left OFF for a time long enough to allow the internal board voltages to discharge sufficiently.**
**If the OFF time is not observed, parts of the board or attached peripherals may work incorrectly or even suffer a reduction of MTBF.**
**The minimum OFF time depends on the implemented PSU model and other electrical factors and needs to be measured individually for each case.**

**NOTICE**

**To protect external power lines of peripheral devices, make sure that the wires have the right diameter to withstand the maximum available current. The enclosure of the peripheral device has to fulfill the fire-protection requirements of IEC/EN62368.**

# 7/ Installation and Setup Procedures

The Board Support Package (BSP) is based on Yocto 2.5 Sumo and uses layers from Yocto, OpenEmbedded, and FSL Community BSP projects.

BSP makes use of proprietary hardware support packages that are covered by NXP SOFTWARE LICENSE AGREEMENT. This agreement explicitly disallows redistribution of covered objects. Because of that, the BSP provides sources and binaries/images for open-source components. So rootfs images to deploy and boot on board must be built manually. Yocto tools completely automate this process – including downloading and integrating restricted NXP packages. Brief build instructions are included into this document; for complete information please refer to Yocto documentation at https://www.yoctoproject.org/documentation.

For reference, BSP archive includes binary kernel and device tree images that have been used for BSP validation. However, for consistency reasons, it is recommended to use kernel and device tree images created by local build.

## 7.1. Building BSP images (rootfs, kernel, device tree)

1. Make sure that your host development system meets the following requirements: https://www.yoctoproject.org/docs/2.5.3/mega-manual/mega-manual.html#detailed-supported-distros

2. Create an empty BSP directory and change to it.

3. Unpack BSP metadata:

```
tar xzf /path/to/sources/sources-base-*.tar.gz
tar xzf /path/to/sources/sources-meta-kontron-sal28-*.tar.gz
```

This will create "sources/" subdirectory populated with metadata layers

4. Set up Yocto build environment:

```
cp sources/meta-kontron-sal28/setup-env ./
source setup-env -m kontron-sal28 -b ./build
```

While this command runs, NXP EULA will be shown. User has to accept it, or BSP build will fail.

5. Once license is accepted, build session is set up in ./build/ subdirectory.

6. Build session could be used to build target system images - which includes kernel image, device tree image and root filesystem image. BSP provides custom image recipe called "sal28-machine-test". It's recommended to start with it. Users already familiar with Yocto can also try building standard Yocto images and/or individual packages.

7. But before building, some extra configuration must be added to "conf/local.conf" file. E.g. "sal28-machine-test" contains binary KEAPI libraries that require agreement with their license. To integrate them into image, following line should be added to "conf/local.conf":

```
LICENSE_FLAGS_WHITELIST += " commercial_libkeapi3 "
```

8. When the build process is completed, the resulted images (kernel, device trees, kernel modules, archived rootfs image and archived sd/usb image) can be found in build/tmp/deploy/images/kontron-sal28/ directory. E.g.:

```
└── kontron-sal28
    ├── Image
    ├── sl28-var2.dtb
    ├── sl28-var34.dtb
    ├── sl28-var2-ads2.dtb
    ├── sl28-var34-ads2.dtb
    ├── sl28-var2-s1914.dtb
    ├── sl28-var34-s1914.dtb
    ├── sl28-var3-ads2-am1280800.dtb
    ├── sl28-var3-ads2-b101uan021.dtb
    ├── modules-kontron-sal28.tgz
    ├── sal28-machine-test-kontron-sal28.tar.gz
    └── sal28-machine-test-kontron-sal28.wic.gz
```

## 7.2. Deploying created images to SD card or USB flash/disk and booting from it

Note: Kernel image, device tree images and kernel modules are automatically integrated into rootfs and sd/usb images.

1. Attach installation media (SD card or USB flash/disk) to Linux host computer and determine a device node by analyzing system logs:

```
dmesg | tail | grep sd
```

Note: an SD/USB storage should greater than 4 GB.

2. Extract a previously built SD/USB image from archive:

```
gunzip sal28-machine-test-kontron-sal28.wic.gz
```

Note: more information about WIC images can be found in official Yocto documentation:
https://www.yoctoproject.org/docs/2.5.3/dev-manual/dev-manual.html#creating-partitioned-images-using-wic

3. Deploy this image to SD/USB storage using a dd command. E.g.:

```
dd if=sal28-machine-test-kontron-sal28.wic of=/dev/sdb bs=4M oflag=direct
```

Note: all information on SD/USB storage will be erased!

4. Configure serial connection on SER1 port, then connect the installation media to SMARC-sAL28 and power on/reset the board.

5. (Option #1: semi-automatic boot) When a U-Boot prompt will appear, a boot device and device tree should be selected by setting following variables:

boot_targets, which can be set to:

- mmc0: to boot from SD;
- mmc1: to boot from eMMC;
- nvme0: to boot from NVMe disk;
- usb0: to boot from USB storage.
- carrier, which can be set to:
- ads2: if variant 3 or variant 4 with Kontron SMARC Evaluation Carrier 2.0 is used;
- s1914: if variant 3 or variant 4 with Kontron KBox A-230-LS Carrier is used;
- var2_on_ads2: if variant 2 on Kontron SMARC Evaluation Carrier 2.0 is used.

E.g. to boot variant 3 on Kontron SMARC Evaluation Carrier 2.0 from SD a following commands should be executed:

```
setenv boot_targets mmc0
setenv carrier ads2
run bootcmd
```

6. (Option #2: manual boot) Interrupt the boot process and check U-boot environment variables with "printenv". If needed, modify paths to kernel image and device tree table. E.g:

```
setenv image /Image
setenv fdt_file /sl28-var34-ads2.dtb
```

To boot the board, execute the following commands depending on which type of installation media is used:

- For USB flash/disk:

```
setenv bootargs root=/dev/sda2 rootwait default_hugepagesz=2m hugepagesz=2m hugepages=256 video=1920x1080
cma=256M
usb start
usb dev 0
fatload usb 0:1 ${fdt_addr_r} ${fdt_file}
fatload usb 0:1 ${kernel_addr_r} ${image}
run hdpload
booti ${kernel_addr_r} - ${fdt_addr_r}
```

- For SD card:

```
setenv bootargs root=/dev/mmcblk0p2 rootwait default_hugepagesz=2m hugepagesz=2m hugepages=256
video=1920x1080 cma=256M
mmc dev 0
```

```
fatload mmc 0:1 ${fdt_addr_r} ${fdt_file}
fatload mmc 0:1 ${kernel_addr_r} ${image}
run hdpload
booti ${kernel_addr_r} - ${fdt_addr_r}
```

7. After board booted up, login as user root. No password is needed.

For more information on U-boot commands please refer to U-boot user manual here:
http://www.denx.de/wiki/DULG/Manual

## 7.3. Booting from NFS server

Note: Setting up NFS booting is highly dependent on Linux distribution used on host. For more details about setting up NFS, DHCP and TFTP daemons consult your distribution documentation.

1. On Linux host computer create a directory for NFS root (say /nfsroot) and extract the rootfs image into it. E.g.:

```
tar xpf /path/to/sal28-machine-test-kontron-sal28.tar.gz -C /nfsroot
```

2. Add NFS root directory to /etc/exports and start NFS server.

3. Copy kernel from extracted rootfs image (Image) into TFTP server root directory ("/var/lib/tftpboot" or "/tftpboot" or "/srv/tftp" depending on Linux distribution). Configure and start TFTP server.

4. Copy an appropriate device tree image (e.g. sl28-var34.dtb) into TFTP server root directory.

5. Configure DHCP server to provide IP configuration for SMARC-sAL28 board.

6. Configure serial connection

7. Power on the board. Interrupt autoboot process by pressing any key on serial console and check U-boot environment variables with "printenv". If needed, modify corresponding variables with setenv command and boot Linux from TFTP server on host by executing:

```
setenv bootargs default_hugepagesz=2m hugepagesz=2m hugepages=256 video=1920x1080-32@60 cma=256M
root=/dev/nfs rw ip=dhcp nfsroot=<host ip>:<path to unpacked rootfs on host>,v3,tcp
setenv serverip <host ip>
setenv ipaddr <sal28 ip>
setenv fdt_file <device tree image copied to tftp>
setenv image <kernel copied to tftp>
tftp ${fdt_addr_r} ${fdt_file}
tftp ${kernel_addr_r} ${image}
booti ${kernel_addr_r} - ${fdt_addr_r}
```

For example:

```
setenv bootargs default_hugepagesz=2m hugepagesz=2m hugepages=256 video=1920x1080-32@60 cma=256M
root=/dev/nfs rw ip=dhcp nfsroot=10.42.0.1:/media/nfsroot/sal28,v3,tcp
setenv serverip 192.168.99.1
setenv ipaddr 192.168.99.101
setenv fdt_file sl28-var34-ads2.dtb
setenv image Image
tftp ${fdt_addr_r} ${fdt_file}
tftp ${kernel_addr_r} ${image}
booti ${kernel_addr_r} - ${fdt_addr_r}
```

8. After board booted up, login as user root. No password is needed.

## 7.4. Deploying created images to on-board eMMC and booting from it

Note: Kernel image, device tree images and kernel modules are automatically built into rootfs image.

1. Boot SMARC-sAL28 either from SD card, USB flash/disk or from NFS as was described above.

2. Deploy the extracted SD/USB image (a wic file) to another USB flash/disk and connect it to the booted SMARC-sAL28 system.

3. Mirror the image from the inserted SD/USB storage to the eMMC device:

```
dd if=/path/to/sal28-machine-test-kontron-sal28.wic of=/dev/mmcblk1 bs=4M oflag=direct
```

Note: all information on eMMC will be erased!

4. Reboot SMARC-sAL28

5. Interrupt the boot process and check U-boot environment variables with “printenv”. If needed, modify paths to kernel image and device tree table. E.g:

```
setenv image /Image
setenv fdt_file /sl28-var34-ads2.dtb
```

6. Execute the following commands:

```
setenv bootargs root=/dev/mmcblk1p2 rootwait default_hugepagesz=2m hugepagesz=2m hugepages=256
video=1920x1080 cma=256M
mmc dev 1
fatload mmc 1:1 ${fdt_addr_r} ${fdt_file}
fatload mmc 1:1 ${kernel_addr_r} ${image}
run hdpload
booti ${kernel_addr_r} - ${fdt_addr_r}
```

7. After board booted up, login as user root. No password is needed.

# 8/ Implementation Notes

## 8.1. GPIO

SMARC GPIO0-GPIO11 lines are mapped in Linux  in the following way:

**Table 27: GPIO**

| Name | Legacy interface: "/sys/class/gpio" | Modern interface: "/dev/gpiochip" |
|---|---|---|
| GPIO0 | gpio400 | GPIO0_CAM0_PWR_N |
| GPIO1 | gpio401 | GPIO1_CAM1_PWR_N |
| GPIO2 | gpio402 | GPIO2_CAM0_RST_N |
| GPIO3 | gpio403 | GPIO3_CAM1_RST_N |
| GPIO4 | gpio404 | GPIO4_HDA_RST_N |
| GPIO5 | gpio405 | GPIO5_PWM_OUT |
| GPIO6 | gpio406 | GPIO6_TACHIN |
| GPIO7 | gpio407 | GPIO7 |
| GPIO8 | gpio392 | GPIO8 |
| GPIO9 | gpio393 | GPIO9 |
| GPIO10 | gpio394 | GPIO10 |
| GPIO11 | gpio395 | GPIO11 |

These GPIOs could be controlled either over sysfs (legacy approach), as documented in https://elixir.bootlin.com/linux/v4.14/source/Documentation/gpio/sysfs.txt . For example, following shell script blinks carrier's LED connected to GPIO5 line:

```
echo 405 > /sys/class/gpio/export
echo out > /sys/class/gpio/gpio405/direction
while true; do
echo 0 > /sys/class/gpio/gpio405/value
sleep 1
echo 1 > /sys/class/gpio/gpio405/value
sleep 1
done
```

Or via modern "/dev/gpiochip" interface, information about which and corresponding examples/tools can be found at following links:

https://elixir.bootlin.com/linux/v4.14/source/include/uapi/linux/gpio.h

https://elixir.bootlin.com/linux/v4.14/source/tools/gpio

https://git.kernel.org/pub/scm/libs/libgpiod/libgpiod.git/tree/README?h=v1.4.x

**NOTICE** **GPIO5 and GPIO6 are shared with PWM_OUT and TACHIN signals, so one function (fan, gpio) can be used at the same time.**

Also the gpio lines support interrupt handling from userspace. For this purpose the attributes "edge" and "value" in sysfs should be used. There is a simple program in C language which gratefully illustrate how this interface may be used by developers: https://developer.ridgerun.com/wiki/index.php?title=Gpio-int-test.c

Plus a gpiomon tool from libgpiod tools, which is provided as part of the BSP, can be used to monitor the GPIO interrupts. E.g.:

```
# gpiofind GPIO7
gpiochip4 7
# gpiomon gpiochip4 7
```

## 8.2. UART

SMARC serial ports are enabled via UART ports on LS1028A SoC. Under Linux:

- SER0 maps to /dev/ttyLP0 Notes: RTS and CTS are available;
- SER1 maps to /dev/ttyS0 Notes: RX and TX only, Console port;
- SER3 maps to /dev/ttyS1 Notes: RX and TX only

LP-UART supports operation in half-duplex mode. For example, in case of KBox A-230-LS carrier board following options can be configured via device tree:

- RS232:

```
&cpld_gpio1 {
     rs485-gpio {
         gpio-hog;
         gpios = <0 GPIO_ACTIVE_HIGH>;
         output-low;
     };
     rs232-gpio {
         gpio-hog;
         gpios = <1 GPIO_ACTIVE_HIGH>;
         output-low;
      };
};
&lpuart1 {
};
```

- RS485 half-duplex (2-wires):

```
&cpld_gpio1 {
     rs485-gpio {
         gpio-hog;
         gpios = <0 GPIO_ACTIVE_HIGH>;
         output-high;
     };
     rs232-gpio {
         gpio-hog;
         gpios = <1 GPIO_ACTIVE_HIGH>;
         output-high;
      };
};
&lpuart1 {
    rs485,rts-low-polarity;
    linux,rs485-enabled-at-boot-time;
};
```

- RS485 full-duplex (4-wires):

```
&cpld_gpio1 {
     rs485-gpio {
         gpio-hog;
         gpios = <0 GPIO_ACTIVE_HIGH>;
         output-low;
     };
     rs232-gpio {
         gpio-hog;
         gpios = <1 GPIO_ACTIVE_HIGH>;
         output-high;
      };
```

```
};
&lpuart1 {
    rs485,rts-low-polarity;
    linux,rs485-enabled-at-boot-time;
};
```

## 8.3. PCI

In case if the optimization/customization of the BSP kernel, it is necessary to make sure that CONFIG_PCIE_DW_PLAT is still enabled in kernel config. Otherwise the PCIe controller won't be initialized properly and particular PCIe Gen2 devices won't be enumerated and detected automatically during boot.

## 8.4. I2C Buses

I2C_PM and I2C_GP buses on SMARC carrier are mapped to i2c-1 and i2c-2 devices accordingly:

```
# i2cdetect -l
i2c-1   i2c             2030000.i2c                             I2C adapter
i2c-2   i2c             2040000.i2c                             I2C adapter
```

These devices can be accessed using a standard dev-interface API:
https://elixir.bootlin.com/linux/v4.14/source/Documentation/i2c/dev-interface

## 8.5. SPI Buses

SPI0 on SMARC connector is an "ordinary" SPI bus governed by Freescale DSPI controller/driver. To make this bus available in KEAPI, an spidev driver is bound in sl28.dts device tree file:

```
&dspi2 {
bus-num = <2>;
status = "okay";
dspidev@0 {
compatible = "spidev";
reg = <0>;
spi-max-frequency = <50000000>;
};
};
```

As a result, the bus can be accessed via standard dev-interface as /dev/spidev2:
https://elixir.bootlin.com/linux/v4.14/source/Documentation/spi/spidev

ESPI on SMARC connector is handled by Flex SPI controller/driver. This controller is optimized for SPI-NOR flash reading usecase and is not suitable for generic SPI transfers of arbitrary length. So devices other than flash are not supported.

The BSP provides an MTD interface for SPI-NOR flash chips connected to ESPI bus. User needs to adjust DTS file and describe connected chips in fspi node in the device tree. Here's example DTS snippet for Winbond W25Q128FW chip:

```
&fspi {
        flash1: w25q128fw@1 {
                # address-cells = <1>;
                # size-cells = <1>;
                compatible = "jedec,spi-nor";
                m25p,fast-read;
                spi-max-frequency = <30000000>;
                reg = <1>;
                /* The following setting enables 1-1-8 (CMD-ADDR-DATA) mode */
                spi-rx-bus-width = <4>; /* 4 SPI Rx lines */
                spi-tx-bus-width = <4>; /* 4 SPI Tx line */
                status = "okay";
        };
};
```

reg property should correspond to cs: 0 for ESPI_CS0#, 1 for ESPI_CS1#

**NOTICE** The BSP provides a read-only access to on-module SPI flash with U-Boot boot loader.

The BSP provides a read-only access to on-module SPI flash with U-Boot boot loader, and which is located at ESPI bus at CS0, via MTD interface:

```
mtd0: 00010000 00001000 "rcw"
mtd1: 000f0000 00001000 "failsafe bootloader"
mtd2: 00040000 00001000 "failsafe DP firmware"
mtd3: 000a0000 00001000 "failsafe PPA firmware"
mtd4: 00020000 00001000 "reserved"
mtd5: 00010000 00001000 "configuration store"
mtd6: 000f0000 00001000 "bootloader"
mtd7: 00040000 00001000 "DP firmware"
mtd8: 000a0000 00001000 "PPA firmware"
mtd9: 00020000 00001000 "bootloader environment"
```

## 8.6. Watchdog

Two watchdog devices are supported by the BSP:

- /dev/watchdog0 and /dev/watchdog1 are additional watchdog timers ( /dev/watchdog0 is also available as legacy /dev/watchdog), which correspond to built-in watchdog device in LS1028A SoC;
- /dev/watchdog2 is a main watchdog timer, which corresponds to watchdog device in CPLD. This watchdog device is able to reset the CPU and to assert WDT_TIME_OUT# line on SMARC connector.

Note that KEAPI provides access only to the CPLD watchdog (/dev/watchdog2). But it can be easily changed by adjusting a corresponding config: /etc/keapi/watchdog.conf. Please refer to /etc/keapi/watchdog_cpld.conf and /etc/keapi/watchdog_soc.conf.

## 8.7. CAN

FlexCAN controller controller and corresponding driver support operation in two modes: CAN FD and CAN 2.0. By default a CAN FD mode, which may not be supported by some devices, is activated. To switch to CAN 2.0 mode, following commands can be used:

```
# ifconfig can0 down
# ip link set can0 type can fd off
# ip link set can0 type can bitrate 1000000 #NOTE: bitrate should be adjusted
# ifconfig can0 up
```

## 8.8. Video Output (DP and LVDS)

Depending on type of SMARC-sAL28 module, either DP or LVDS output is supported.

To activate a DP output, following actions should be performed:

- DP firmware should be loaded in U-Boot before loading Linux. i.e. following command should be executed in U-Boot prompt:

  ```
  run hdpload
  ```
- an “ordinary” dtb file (sl28-var34-ads2.dtb) should be loaded;
- an appropriate resolution should be passed to kernel via cmdline, e.g.:

  ```
  default_hugepagesz=2m hugepagesz=2m hugepages=256 video=1920x1080-32@60 cma=256M root=/dev/nfs rw ip=dhcp
  ```
- the same resolution should be defined for HDMI-A-1 output in /etc/xdg/weston/weston.ini, e.g.:

  ```
  [core]
  idle-time=0
  [output]
  name=HDMI-A-1
  mode=1920x1080@60
  [screen-share]
  command=/usr/bin/weston --backend=rdp-backend.so --shell=fullscreen-shell.so --no-clients-resize
  ```
- the list of supported resolution can be found in /var/log/weston.log

In the current version of the BSP, only two LVDS displays are supported: AUO B101UAN02.1 (1920x1200) and AM-1280800N4TZQ (1280x800). The same actions as for DP output above should be performed to activate them, except that a special dtb file should be used: either sl28-var3-ads2-b101uan021.dtb or sl28-var3-ads2-am1280800.dtb depending on the model of connected display.

Instructions and examples how to add support of another LVDS displays will be provided in future versions of the document.

## 8.9. Fan Monitoring and Control

The BSP provides a standard hwmon interface for PWM_OUT and TACHIN signals:

https://elixir.bootlin.com/linux/latest/source/Documentation/hwmon/sysfs-interface.rst#L335

https://elixir.bootlin.com/linux/latest/source/Documentation/hwmon/sysfs-interface.rst#L248

But these signals are shared with GPIO5 and GPIO6:

- GPIO5 pin is configured as GPIO by default, and:
- following commands can be executed to enable PWM_OUT instead:

```
echo 0 > /sys/class/pwm/pwmchip0/export
echo 1 > /sys/class/pwm/pwmchip0/pwm0/enable
```

- to disable PWM_OUT and enable GPIO5 again:

```
echo 0 > /sys/class/pwm/pwmchip0/pwm0/enable
```

- By contrast, GPIO6 pin is visible both as a TACHIN and as GPIO, but only one function (fan, gpio) should be used at a time:
- to disable a hwmon interface for TACHIN, a device tree should be adjusted as follows:

```
fan@b {
            compatible = "kontron,sl28cpld-fan";
            reg = <0xb>;
            status =  "disabled" ;
 };
```

- in case if TACHIN is used, corresponding GPIO pin should be conifgured as INPUT and shouldn't be accessed.

## 8.10. Thermal Management

### 8.10.1. Heatspreader and Cooling Solutions

A heatspreader plate assembly is available from Kontron for the SMARC-sAL28. The heatspreader plate on top of this assembly is NOT a heat sink. The heatspreader works as a thermal interface to be use with a heat sink or external cooling devices.

External cooling must be provided to maintain the heatspreader plate at proper operating temperatures. Under worst-case conditions, the cooling mechanism must maintain an ambient air temperature and the heatspreader plate's surface temperature must remain under the maximum temperature range.

### 8.10.2. Operating with Kontron Heatspreader Plate (HSP) Assembly

The operating temperature defines two requirements:

- Maximum ambient temperature with ambient being the air surrounding the module
- Maximum measurable temperature on any spot on the heatspreader's surface

The heatspreader is tested for the following temperature specifications.

Table 28: Heatspreader Test Temperature Specifications

| Temperature Specification | Validation requirements |
|---|---|
| Commercial Grade | at 60°C HSP temperature the CPU @ 100% load needs to run at nominal frequency |
| Industrial Grade by screening (E2S) | at 85°C HSP temperature the CPU @ 50% load is allowed to start throttling for thermal protection |

### 8.10.3. Operating without Kontron Heatspreader Plate Assembly

The operating temperature is the maximum measurable temperature on any spot on the module's surface.

**NOTICE**

**The CPU is configured, that it starts to throttle its frequency to 647 MHz, when a CPU temperature of 85°C is reached.**

## 8.11. TSN Switch

To evaluate the functionality of TSN switch:

- A Quad PHY should be connected to QSGMI interface, which is routed to PCIE_D pins of SMARC connector. Plus this PHY should be enabled in device tree. In case of Kontron SMARC S1914 carrier board, it can be achieved by loading sl28-*-s1914.dtb.
- When Linux is booted, the interfaces of TSN switch should be brought-up and aggregated into bridge:

```
# ip link add name br0 type bridge
# ifconfig br0 up
# ip link set swp0 master br0
# ip link set swp1 master br0
# ip link set swp2 master br0
# ip link set swp3 master br0
# ip link set swp4 master br0
# ip link set swp5 master br0
# ifconfig swp0 up
# ifconfig swp1 up
# ifconfig swp2 up
# ifconfig swp3 up
# ifconfig swp4 up
# ifconfig swp5 up
# ifconfig eno2 up
# ifconfig eno3 up
```

- Afterwards it should be possible to assign an IP address to br0 device and communicate with SMARC-sAL28 over any port of TSN switch using this IP address:

```
# ifconfig br0 10.42.1.10
# ping 10.42.1.1 -c 5
```

**NOTICE**

**Despite the fact that linuxptp package is integrated into the BSP, the PTP functionality of TSN switch has not been validated yet. For more information about interaction with the TSN switch, please refer to User's Guide for reference Linux BSP for LS1028A from NXP: "Layerscape LS1028A BSP User Guide" or LS1028ABSPUG.pdf.**

# 9/ Bootloader Operation

## 9.1. Copyrights and Licensing of U-Boot

U-Boot is free Software. It is copyrighted by Wolfgang Denk and many others who contributed code. U-Boot can be redistributed and modified under the terms of version 2 of the GNU General Public (GPL V2) License as published by the Free Software Foundation.

Actual source code of mainline U-Boot and authors of the source can be obtained from the git repository at

- git://git.denx.de/u-boot.git

SMARC-sAL28 bootloader sources are derived work from a dedicated version of mainline U-Boot, e.g v2018.07. As bootloader evolves, the root of the derived work might change to a later version.

**NOTICE**

**The source code of U-Boot will be delivered with the standard software package. Additionally the software can be downloaded from Kontron GitHub repository for SMARC-sAL28: https://github.com/kontron/u-boot-smarc-sAL28.git**

## 9.2. Bootloader Quickstart

The SMARC-sAL28 board comes with U-Boot preinstalled on the QSPI flash device. Follow the steps below to gain access to the bootloader command line (CLI) on your host PC.

- Connect your host machine to the carrier port connected with the edge connector SER_0 port of the module. On Kontron SMARC 2.0 carrier this port is named SER_1.
- Start a suitable terminal program on your host and attach it to the port connected with the board's serial interface. Configure the serial line using **115200 baud, 8 data bits, 1 stop bit, no parity**.
- Connect power supply to the carrier and power up.
- When boot messages appear, press any key to stop automatic boot sequence.

After power on, bootloader boot messages will appear as shown below. There is a 2 second boot delay counter that will try to boot linux OS automatically after expiration. Pressing any key will stop the boot delay counter and enter the bootloader CLI

.

```
U-Boot SPL 2018.09-g3b96286ea1 (Oct 01 2019 - 00:05:46 +0000)
Initializing DDR....using raw memory timing
SPI boot
Trying to boot from SPI

U-Boot 2018.09-g3b96286ea1 (Oct 01 2019 - 00:05:46 +0000), Build: 401
SoC:  LS1028A Rev1.0 (0x870b0110)
Clock Configuration:
       CPU0(A72):1300 MHz  CPU1(A72):1300 MHz
       Bus:      400  MHz  DDR:      1600 MT/s
Reset Configuration Word (RCW):
       00000000: 34004010 00000030 00000000 00000000
       00000010: 00000000 008f0000 0030c000 00000000
       00000020: 06200000 00002580 00000000 00019016
       00000030: 00000000 00000048 00000000 00000000
       00000040: 00000000 00000000 00000000 00000000
       00000050: 00000000 00000000 00000000 00000000
       00000060: 00000103 00000000 100e7026 00000000
       00000070: bb580000 00020000
Model: Kontron SMARC-sAL28 Board
       Hardware Variant: Single PHY (3)
       RCW: sl28-3-11_q.bin
```

```
DRAM:  Detected UDIMM Fixed DDR on board
3.9 GiB
DDR    3.9 GiB (DDR3, 32-bit, CL=11, ECC on)
Using SERDES1 Protocol: 47960 (0xbb58)
PCIe0: pcie@3400000 Root Complex: x1 gen2
PCIe1: pcie@3500000 Root Complex: x1 gen3
CPLD:  v17
Waking secondary cores to start from fbd38000
All (2) cores are up.
MMC:   FSL_SDHC: 0, FSL_SDHC: 1
Loading Environment from SPI Flash... SF: Detected w25q32dw with page size 256 Bytes, erase size 64 KiB,
total 4 MiB
OK
In:    serial
Out:   serial
Err:   serial
VPD:   Using device 0x50 on I2C Bus 2
Net:   eth0: enetc#0, eth2: enetc#1, eth8: netc_mdio
Hit any key to stop autoboot:  0
```

## 9.3. Bootloader Commands

The bootloader CLI provides a bunch of powerful commands to control the board, which basically can be grouped into

- Information Commands
- Memory Commands
- Flash Memory Commands
- Execution Control Commands
- Download Commands
- Environment Control Commands
- Flattened Device Tree Support Commands
- Storage Device Control Commands
- File System Support Commands
- Kontron Command Extensions

**Typing "help" at the bootloader command line prompt will show up a list of the commands available. Typing "help <command>" will show specific command help. Further help can be found under https://www.denx.de/wiki/view/DULG/UBoot**

On the SMARC_sAL28 bootloader, the powerful hush shell is enabled, which is similar to Bourne shell and provides features similar to a linux shell:

- Control structures (if … then … else … fi etc.)
- Command line completion
- Command line editing
- Command line history up to 20 entries
- Local environment variables

## 9.4. Kontron Bootloader Command Extensions

Kontron's implementation of U-Boot includes certain enhancements to provide board specific functions. They are not part of standard U-Boot as maintained by DENX. The following table provides a complete listing of all Kontron command extensions on the SMARC-sAL28.

Table 29: Bootloader Command Extensions

| Command | Description |
|---|---|
| kboardinfo | Kontron Board Information - Displays a summary of board and configuration information |
| wdt | Start and control CPLD and LS1028A core0\|1 CPU watchdog |

### 9.4.1. kboardinfo - Kontron Board Information

The "kboardinfo" command shows a summary of board serialization data gathered from the system EEPROM.

```
=> kboardinfo
Manufacturer:        Kontron Europe GmbH
Product name:        SMARC-sAL28
Material number:     51011-0408-13-2-3
Serial number:       USD0C0001
MAC0 (ethaddr):      00:a0:a5:5c:6b:3a
MAC1 (eth1addr):     00:a0:a5:5c:6b:3b
MAC2 (eth2addr):     00:a0:a5:5c:6b:3c
MAC3 (eth3addr):     00:a0:a5:5c:6b:3d
MAC4 (eth4addr):     00:a0:a5:5c:6b:3e
MAC5 (eth5addr):     00:a0:a5:5c:6b:3f
MAC6 (eth6addr):     00:a0:a5:5c:6b:40
MAC7 (eth7addr):     00:a0:a5:5c:6b:41
Manufacturer Date:   08/26/2019
Revision:            A00
Boot Counter:        3362
```

### 9.4.2. Wdt – CPU Watchdog Control

The wdt command is used to control the CPLD and core0/1 LS1028A CPU internal watchdog.

**Syntax:**

```
=> help wdt
wdt - Watchdog sub-system

Usage:
wdt list - list watchdog devices
wdt dev [<name>] - get/set current watchdog device
wdt start <timeout ms> [flags] - start watchdog timer
wdt stop - stop watchdog timer
wdt reset - reset watchdog timer
wdt expire [flags] - expire watchdog timer immediately
```

## 9.5. Bootloader Environment

The bootloader environment is used to control bootloader and OS startup behavior. Environment variables can be used to control boot timing (e.g. bootdelay), interface properties (e.g. baudrate, ethact) or they define memory locations where OS images are stored before boot (e.g. loadaddr, fdt_addr). In addition, bootloader shell commands can be combined to environment scripts.

The redundant bootloader environment is permanently stored in the QSPI flash device at offset 0x3E0000 and 0x3F0000. During bootloader operation, the environment is held in RAM memory and can be modified and written back to persistent storage.

Bootloader commands to modify the environment are summed up under the "env" command group:

- env default [-f] –a [forcibly] reset default environment
- env default [-f] var [...] [forcibly] reset variable(s) to their default values
- env delete [-f] var [...] [forcibly] delete variable(s)
- env edit name edit environment variable
- env exists name tests for existence of variable
- env exists name tests for existence of variable
- env export [-t | -b | -c] [-s size] addr [var ...] export environment
- env grep [-e] [-n | -v | -b] string [...] search environment
- env import [-d] [-t [-r] | -b | -c] addr [size] [var ...] import environment
- env print [-a | name ...] print environment
- env run var [...] run commands in an environment variable
- env save save environment
- env set [-f] name [arg ...]

However, the legacy commands for environment handling are still available:

- "setenv",
- "editenv",
- "printenv"
- "saveenv".

U-Boot standard environment variables are set up for the SMARC_sAL28 module as shown below.

**Table 30: Standard Environment Variables**

| Variable | Value | Description |
|---|---|---|
| baudrate | 115200 | Serial line baudrate |
| bootcmd | run hdpload; run distro_bootcmd | Try booting from devices defined in the boot_targets variable |
| bootdelay | 2 | Wait 2 seconds before executing bootcmd |
| boot_targets | mmc1 mmc0 nvme0 usb0 dhcp pxe | Boot devices used by distro_bootcmd to boot from |
| loadaddr | 0x81000000 | Default memory location for OS boot |

A typical user modification would be to set the variable "bootcmd" to change OS boot commands.

## 9.6. Bootloader Environment Update

On the SMARC-sAL28 it is possible to update the U-Boot environment separately.

This enables the user to either update from a previous version of the official Kontron sAL28 U-Boot environment (default U-Boot settings), or restore the default in case of problems.

Update procedure:

- Download the official sAL28 U-Boot environment from the Kontron EMD Customer Section.
- Put the file into the root directory of a FAT or EXT formatted USB drive.
- Start the sAL28 system and stop the boot process at the U-Boot prompt.
- Run the following commands to load the file and flash it into the correct flash memory address (example for R10):

```
usb start && load usb 0:1 $loadaddr NXP_LS1028-env-r10.bin
sf probe && sf update $loadaddr 0x3e0000 $filesize
```

- After reset the updated environment will be active.

## 9.7. Bootloader Mass Storage Support

U-Boot provides support to read and write from mass storage devices like

- QSPI flash
- SD card
- USB thumb device

### 9.7.1. QSPI flash

QSPI flash is accessed using the "sf" command

**Example:** Load one sector (64K) from SPI flash

```
=> sf probe 0
=> sf read ${loadaddr} 0 10000
```

### 9.7.2. SD Card and eMMC Devices

eMMC and SD card are accessed using the "mmc" command

**Example:** Load 256 blocks from eMMC

```
=> mmc dev 1
=> mmc read ${loadaddr} 0 100
```

### 9.7.3. USB Storage Device

USB storage devices are accessed using "usb" command

**Example:** Load bootloader update file from USB thumb device

```
=> usb start
=> usb dev 0
=> fatload usb 0:1 update_NXP LS1028_spl/u-boot-NXP LS1028_spl.bin
```

## 9.8. Bootloader File System Support

U-Boot for the SMARC_sAL28 provides support for FAT and EXT4 file systems. EXT4 support also includes EXT2 and EXT3 formatted file systems. There are file system specific commands available to list file system contents (ext2ls, fatls) and load a given file into board memory (ext2load, fatload). However, U-Boot also provides generic commands ("ls" and "load"), that will detect the file system on the device and use appropriate file system functions automatically.

**Example:** Show/boot folder contents from SD card file system

```
=> ls mmc 0:1 /boot
<DIR>       4096 .
<DIR>       4096 ..
<SYM>         48 imx7d-sAL28-id101-m4.dtb
          44034 devicetree-zImage-imx7d-sAL28-id101-m4.dtb
          43986 devicetree-zImage-imx7d-sAL28-id101.dtb
<SYM>         33 zImage
<SYM>         45 imx7d-sAL28-id101.dtb
<SYM>         45 imx7s-sAL28-id101.dtb
         6376512 zImage-4.1.29-fslc+g59b38c3
          43998 devicetree-zImage-imx7s-sAL28-id101.dtb

=> load mmc 0:1 ${loadaddr} /boot/zImage
6376512 bytes read in 536 ms (11.3 MiB/s)
```

## 9.9. Bootloader Network Support

U-Boot provides support for both onboard Ethernet interfaces. The current interface can be selected by setting "ethact" environment variable to either “enetc#0” or “enetc#1”.

Board specific MAC addresses are read from EEPROM during startup and environment variables are set automatically. In case EEPROM contents is missing or corrupted, a "random" MAC address will be set to "ethaddr"

In case that the current network interface is attached to a network providing a DHCP server, an IP address can be gathered using "bootp" or "dhcp" commands.

After that, a file from a tftp server can be copied to memory using the "tftpboot" command.

**Example:**

```
=> bootp
=> tftpboot ${loadaddr} <filename>
```

## 9.10. Bootloader Boot Counter

The module EEPROM device contents implements a SMBIOS Running-time data block (type 161) as defined in the KEU EEPROM Specification Rev. 1.4. The running-time data block structure implements a 64bit boot counter. U-Boot on the SMARC_sAL28 module will read the current boot counter value and increment it on every boot cycle. Current boot counter is shown as part of the information shown by the "kboardinfo" command (see description of kboardinfo).

## 9.11. U-boot Files for the Kontron SMARC sAL28 Module on Github.com

You can find the last program code under https://github.com/kontron/u-boot-smarc-sAL28.git.

# 10/ Technical Support

For technical support contact our Support Department:

E-mail: support@kontron.com
Phone: +49-821-4086-888

Make sure you have the following information available when you call:

Product ID Number (PN),
Serial Number (SN)

**The serial number can be found on the Type Label, located on the product's rear side.**

Be ready to explain the nature of your problem to the service technician.

## 10.1. Warranty

Due to their limited service life, parts that by their nature are subject to a particularly high degree of wear (wearing parts) are excluded from the warranty beyond that provided by law. This applies to the CMOS battery, for example.

**If there is a protection label on your product, then the warranty is lost if the product is opened.**

## 10.2. Returning Defective Merchandise

All equipment returned to Kontron must have a Return of Material Authorization (RMA) number assigned exclusively by Kontron. Kontron cannot be held responsible for any loss or damage caused to the equipment received without an RMA number. The buyer accepts responsibility for all freight charges for the return of goods to Kontron's designated facility. Kontron will pay the return freight charges back to the buyer's location in the event that the equipment is repaired or replaced within the stipulated warranty period. Follow these steps before returning any product to Kontron.

1. Visit the RMA Information website:
http://www.kontron.com/support-and-services/support/rma-information

   Download the RMA Request sheet for **Kontron Europe GmbH** and fill out the form. Take care to include a short detailed description of the observed problem or failure and to include the product identification Information (Name of product, Product number and Serial number). If a delivery includes more than one product, fill out the above information in the RMA Request form for each product.

2. Send the completed RMA-Request form to the fax or email address given below at Kontron Europe GmbH. Kontron will provide an RMA-Number.

   Kontron Europe GmbH
   RMA Support
   Phone: +49 (0) 821 4086-0
   Fax: +49 (0) 821 4086 111
   Email: service@kontron.com

3. The goods for repair must be packed properly for shipping, considering shock and ESD protection.

**Goods returned to Kontron Europe GmbH in non-proper packaging will be considered as customer caused faults and cannot be accepted as warranty repairs.**

4. Include the RMA-Number with the shipping paperwork and send the product to the delivery address provided in the RMA form or received from Kontron RMA Support.

# List of Acronyms

| | |
|---|---|
| CPLD | Complex Programmable Logic Devices |
| CSI | Camera Serial Interface |
| DTE | Data Terminal Equipment |
| DSI | Display Serial Interface |
| DCE | Data Communications Equipment |
| eCSPI | enhanced Configurable Synchronous Programmable serial Interface |
| eCSPI | enhanced Configurable Synchronous Programmable serial Interface |
| eDP | embedded Display Port |
| EMC | Electromagnetic Compatibility |
| EMI | Electromagnetic Interference |
| eMMC | embedded Multimedia Card |
| EPDC | Electronic Paper Display Controller |
| ESD | Electrostatic Discharge |
| GPIO | General-purpose input/output |
| HDA | High Definition Audio |
| HDMI | Integrated High Definition Multimedia Interface |
| I2S | Inter-IC Sound |
| KPP | Key Pad Port |
| LPDDR | Low Power DDR |
| LVDS | Low Voltage Differential Signalling |
| MIPI | Mobile Industry Processor Interface |
| MLC | Multi-level Cell |
| pSLC | pseudo Single Level Cell |
| SDIO | Secure Digital Input Output |
| SMARC | Smart Mobility ARChitecture |
| SMBus | System Management Bus |
| SoC | System on Chip |
| TPM | Trusted Platform Module |
| UART | Universal Asynchronous Receiver Transmitter |

## About Kontron – Member of the S&T Group

Kontron is a global leader in Embedded Computing Technology (ECT). As a part of technology group S&T, Kontron offers a combined portfolio of secure hardware, middleware and services for Internet of Things (IoT) and Industry 4.0 applications. With its standard products and tailor-made solutions based on highly reliable state-of-the-art embedded technologies, Kontron provides secure and innovative applications for a variety of industries. As a result, customers benefit from accelerated time-to-market, reduced total cost of ownership, product longevity and the best fully integrated applications overall.

For more information, please visit: **http://www.kontron.com/**

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